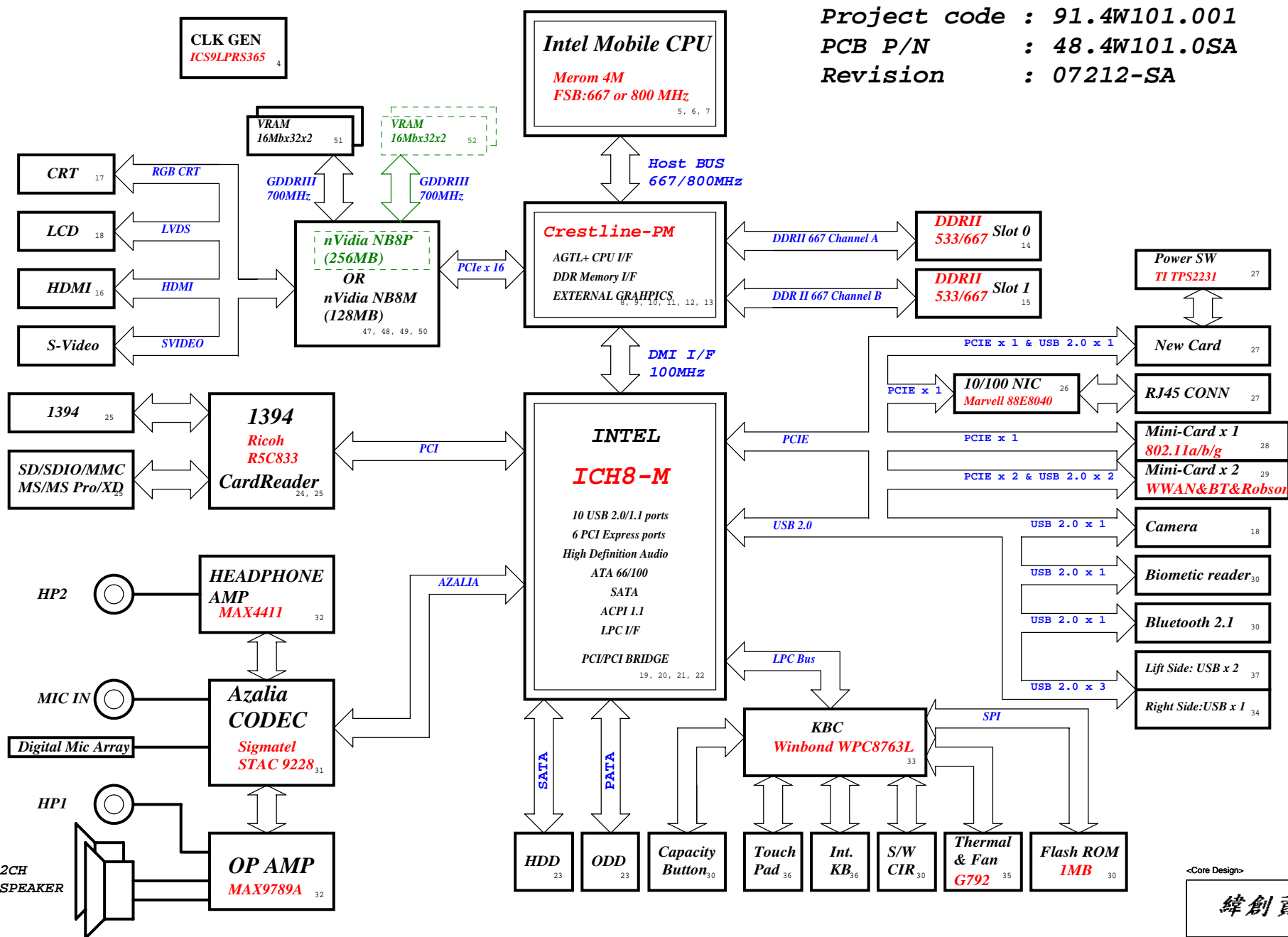


Hawke Intel Discrete Block Diagram

Project code : 91.4W101.001

PCB P/N : 48.4W101.0SA

Revision : 07212-SA



BATTERY CHARGER	
MAX8731A 38	
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT
SYSTEM DC/DC	
TPS51120 39	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5
SYSTEM DC/DC	
TPS5117 42, 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
SYSTEM DC/DC	
TPS51100 44	
INPUTS	OUTPUTS
1D8V_S3	0D9V_S3
SYSTEM DC/DC	
RT9018 44	
INPUTS	OUTPUTS
1D8V_S3 1D8V_S3	1D5V_S0 1D25V_S0
VGA DC/DC	
TPS5117 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFX_CORE_S0
CPU DC/DC	
ISL6262A 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
PCB LAYER	
L1:TOP	
L2:GND	
L3:Signal	
L4:Signal	
L5:VCC	
L6:Singal	
L7:GND	
L8:BOT	

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

	Title
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System Block Diagram

Size
A3

Document Number

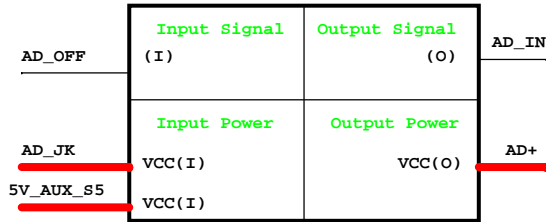
Hawke-Intel

Rev

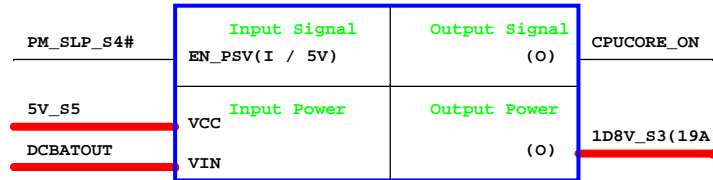
Date: Tuesday, May 08, 2007

Sheet 1 of 55

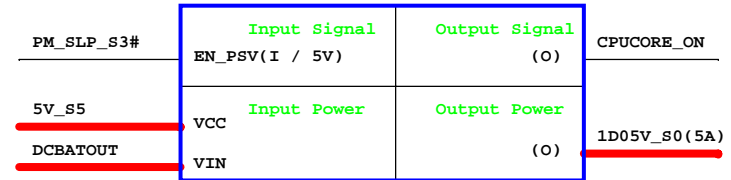
Adapter



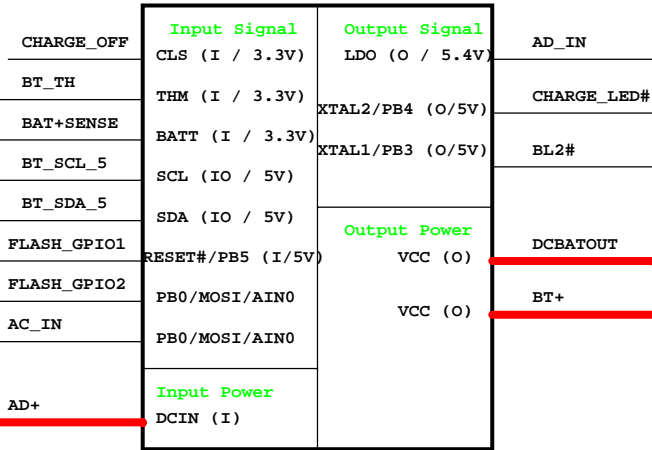
TPS51117 1D8V



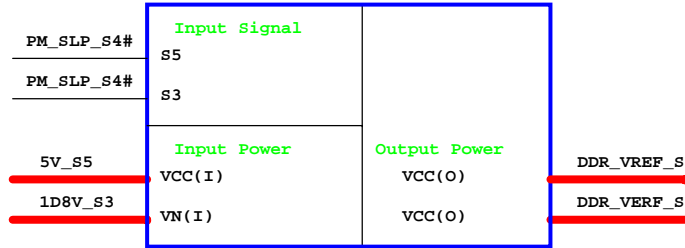
TPS51117 1D05V



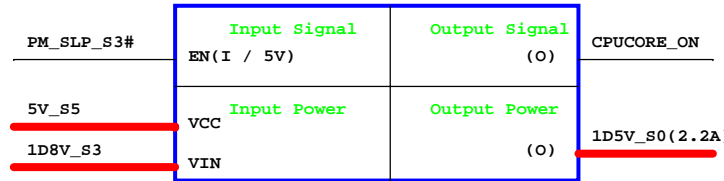
Charger_ISL6255



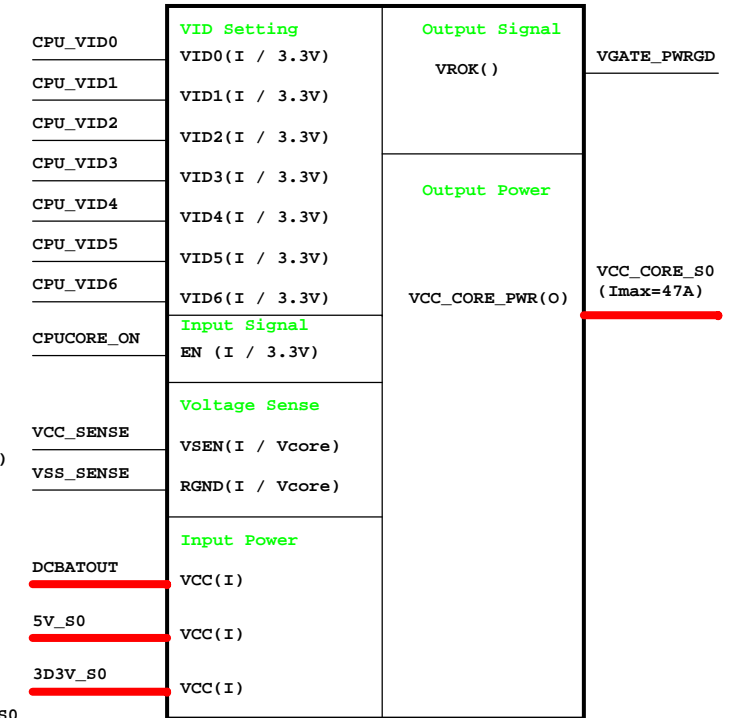
TI TPS51100 0.9V/DDR_VREF_S3



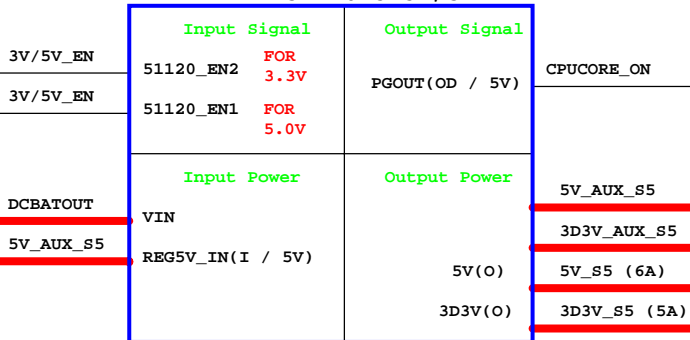
RT9018A 1D5V



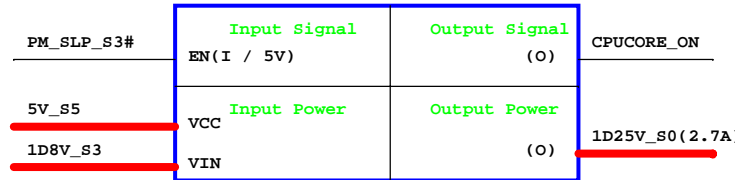
ISL6262A CPU_CORE



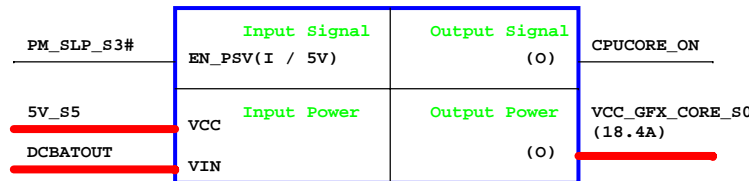
TI TPS51120 3D3V/5V



RT9018A 1D25V



TPS51117 VGA_CORE



<Core Design>

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWB BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable.Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP	TP3	AZ_DOUT	ICH
0	0	0	RSVD
0	1	1	Enter XOR Chain
1	0	0	Normal Operation(default)
1	1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low	high
low	low	high
high	low	high

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
High	High	Low
Low	High	Low

integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable
High	High	Low
Low	High	Low

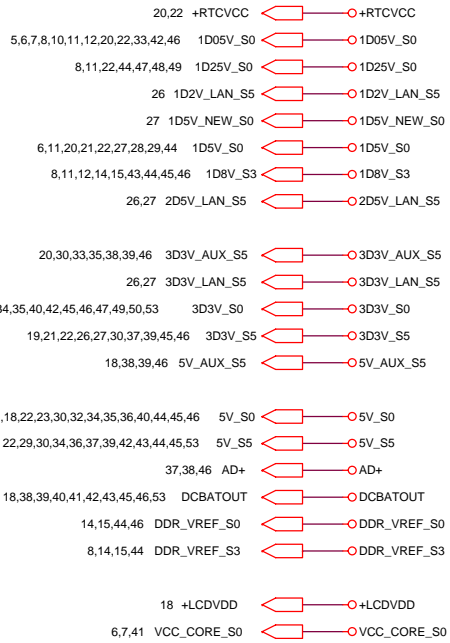
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
Low	Low
High	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



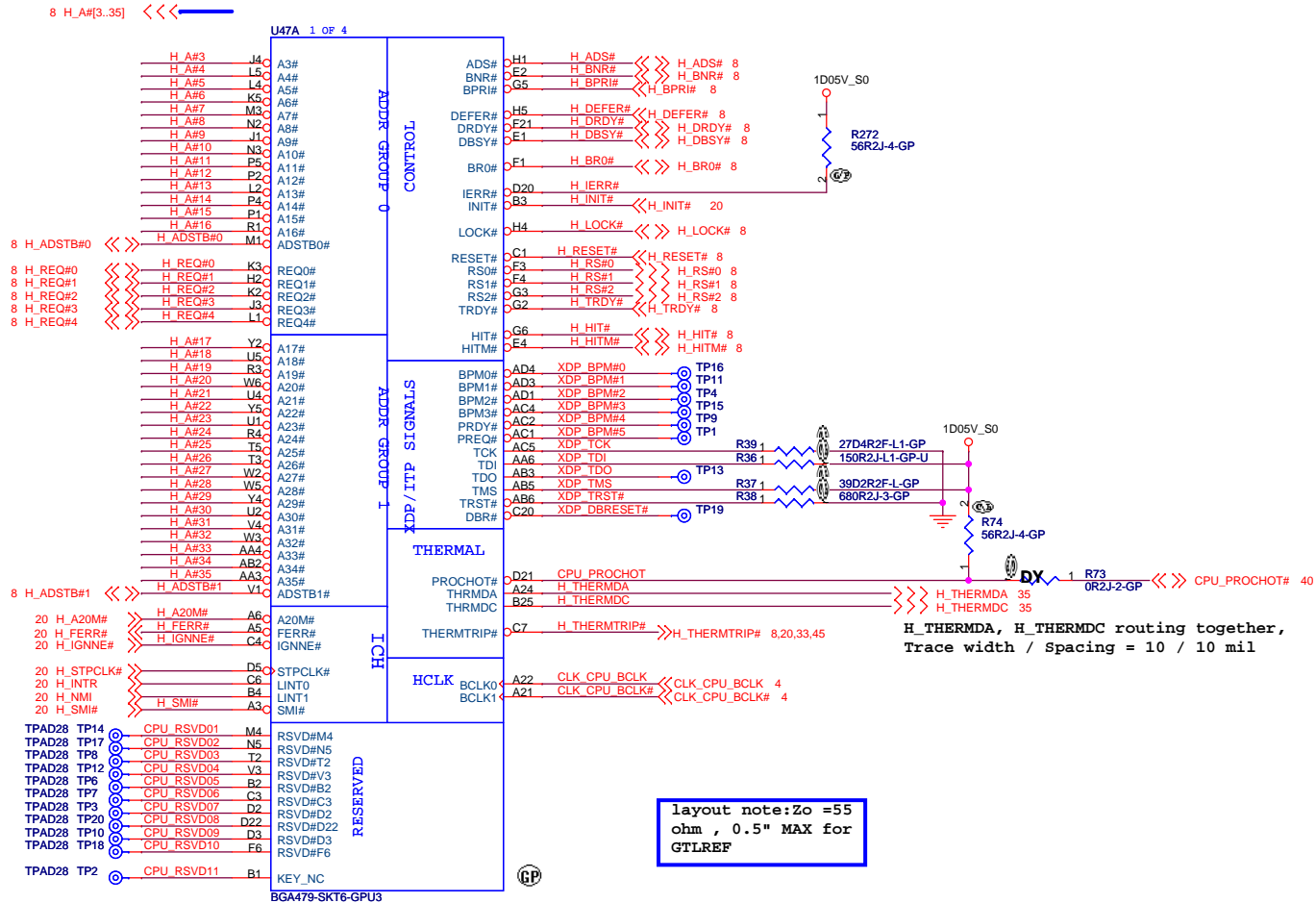
INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 8 Low Power PCI Express	Normal	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled
CFG 19 DMI Lane Reserved	Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present	SDVO Card Present
CFG 12 CFG 13 LL(00)	XOR/ALL-Z Reserved	
LH(01)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HH(11)	Normal Operation	

<Core Design>

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Title		
Table of Content		
Size A3	Document Number	Rev
	Hawke-Intel	SA
Date: Tuesday, May 08, 2007	Sheet 3	of 55



Change to 62.10040.221 04/12 '07

<Core Design>

8 H_D#[0.63] <<>>

<<>>

8 H_DSTBN#0
8 H_DSTBP#0
8 H_DINV#0

8 H_DSTBN#1
8 H_DSTBP#1
8 H_DINV#1

4.8 CPU_BSEL0
4.8 CPU_BSEL1
4.8 CPU_BSEL2

PLACE C617 close to the TEST4 PIN,
make sure TEST3,TEST4,TEST5 trace
routing is reference to GND and
away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor Placed
within 0.5" of CPU
pin. Trace should
be at least 25 mils
away from any other
toggling signal .
COMP[0,2] trace
width is 18 mils.
COMP[1,3] trace
width is 4 mils .

VCC_CORE_S0

VCC_CORE_S0

layout note:
place C618 near
PIN B26

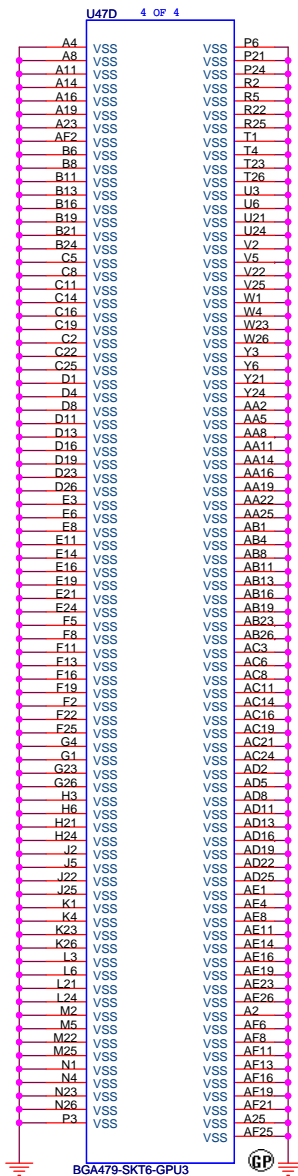
Length match within
25 mils . The trace
width/space/other is
20/7/25 .

Close to CPU pin
within 500mils

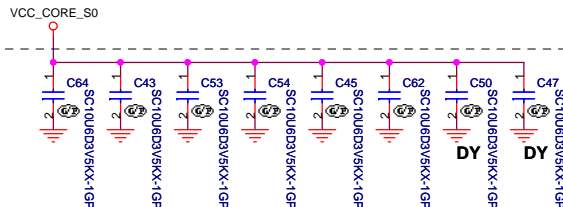
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

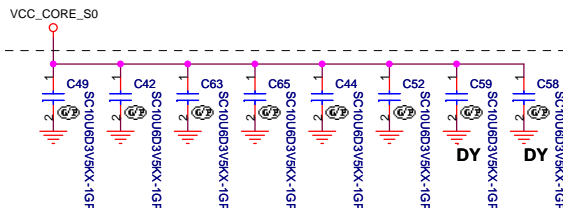
Title			Meron(2/3)-AGTL+PWR		
Size	Document Number	Hawke-Intel			Rev
A3					SA
Date:	Tuesday, May 08, 2007	Sheet	6	of	55



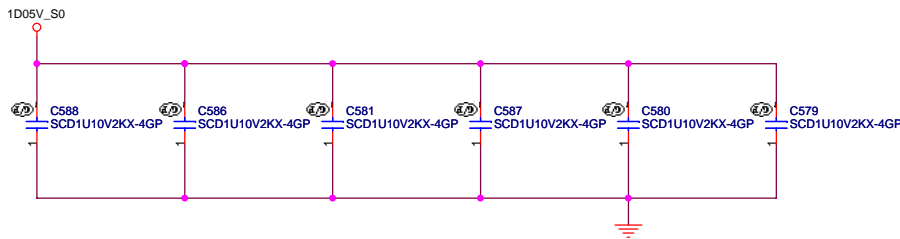
Place these capacitors on L1
(North side ,Secondary Layer)



Place these capacitors on L1
(North side ,Secondary Layer)



Mid Frequenced
Decoupling

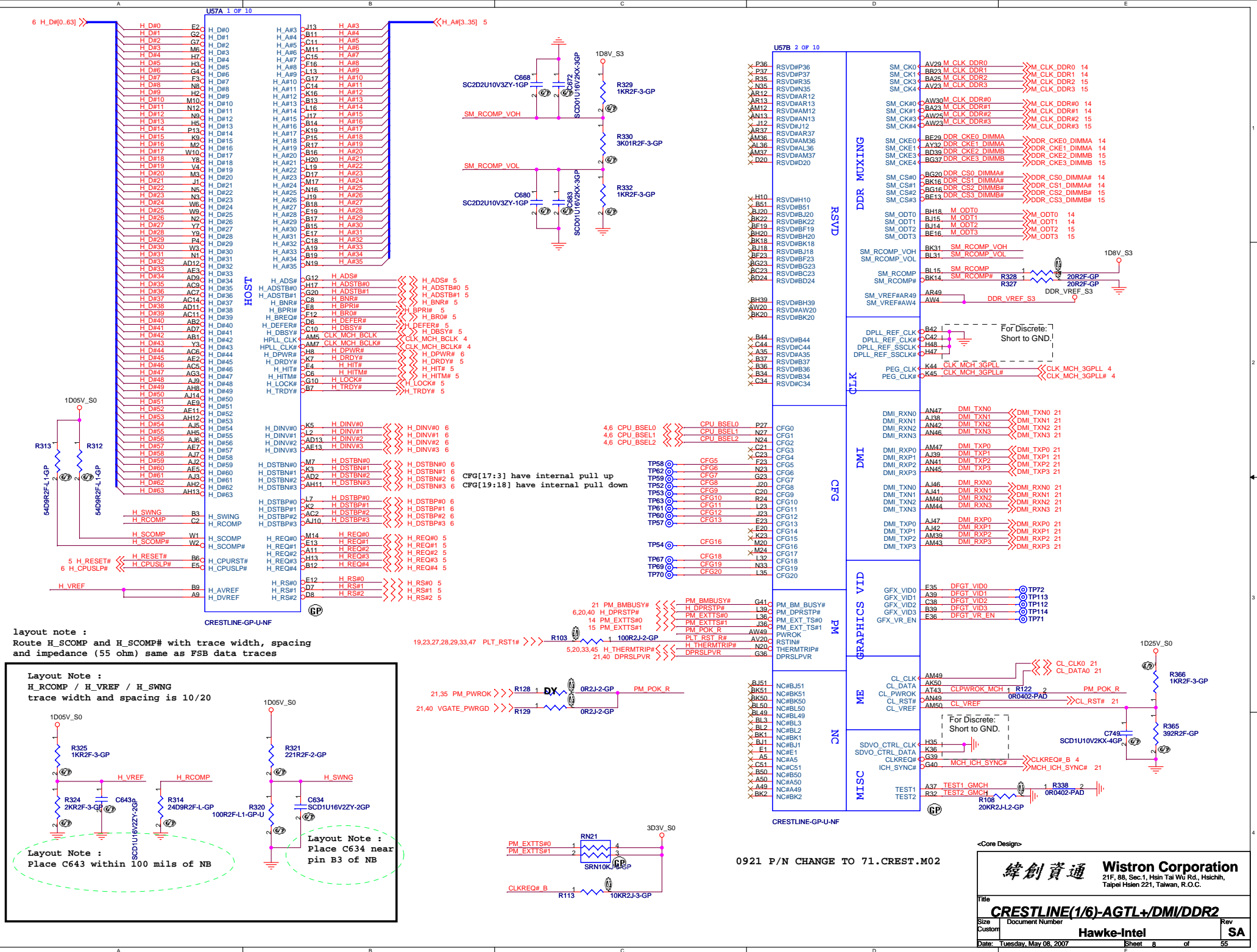


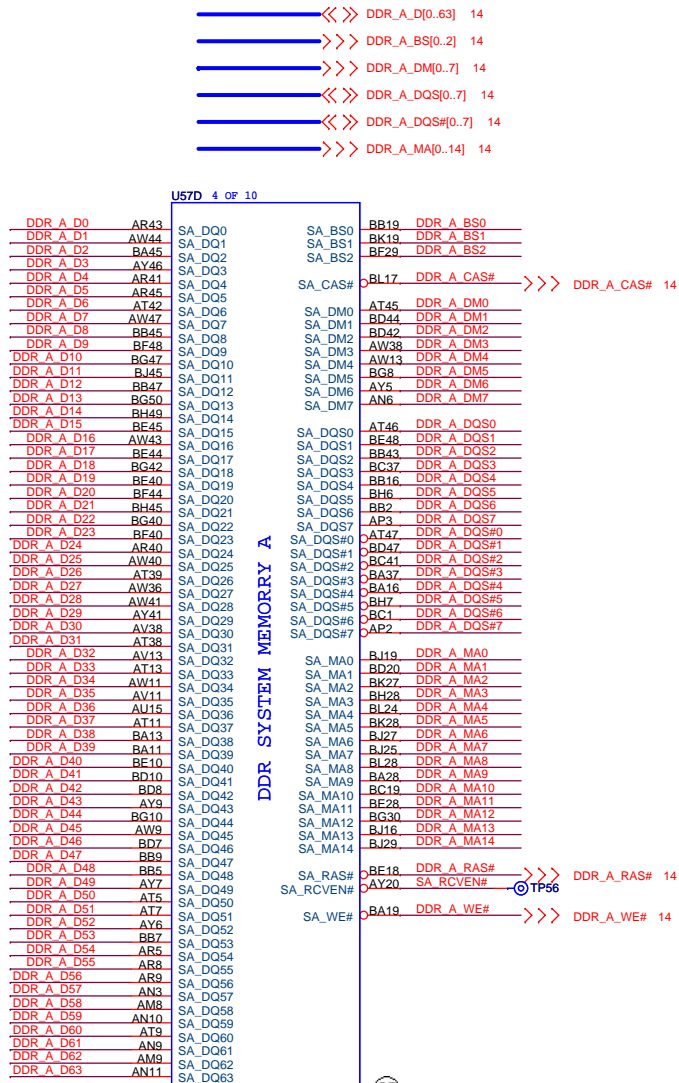
Place these
inside socket
cavity on L1
(North side
Secondary)

<Core Design>

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Title		
Meron(3/3)-GND&Bypass		
Size	Document Number	Rev
A3	Hawke-Intel	SA
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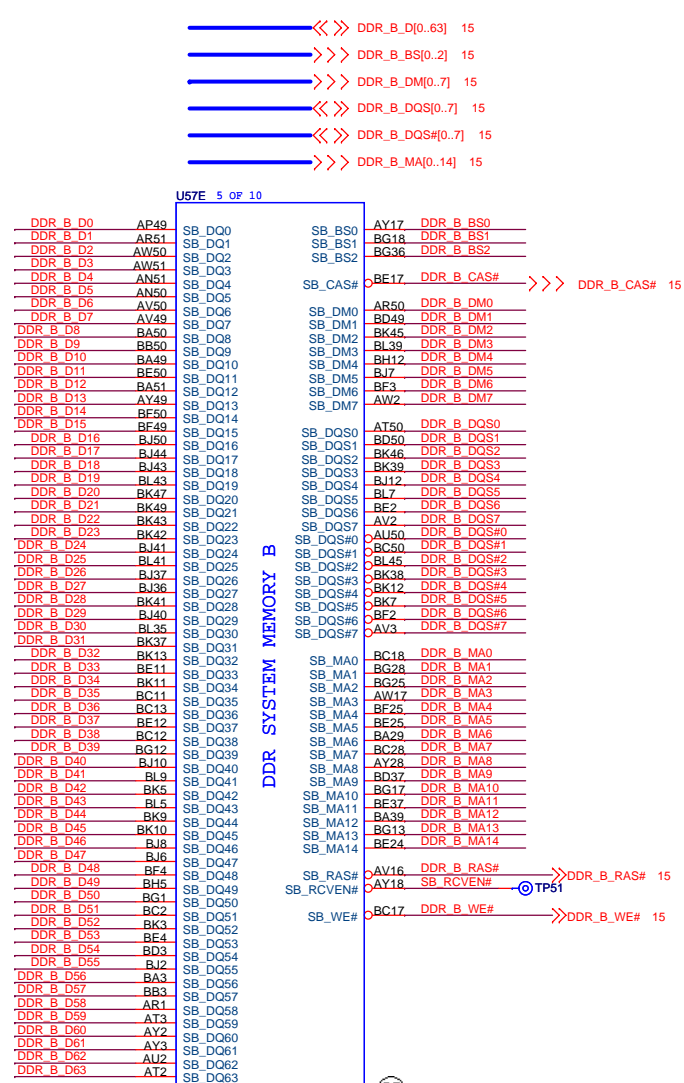




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DDR SYSTEM MEMORY A

CRESTLINE-GP-U-NF



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DDR SYSTEM MEMORY B

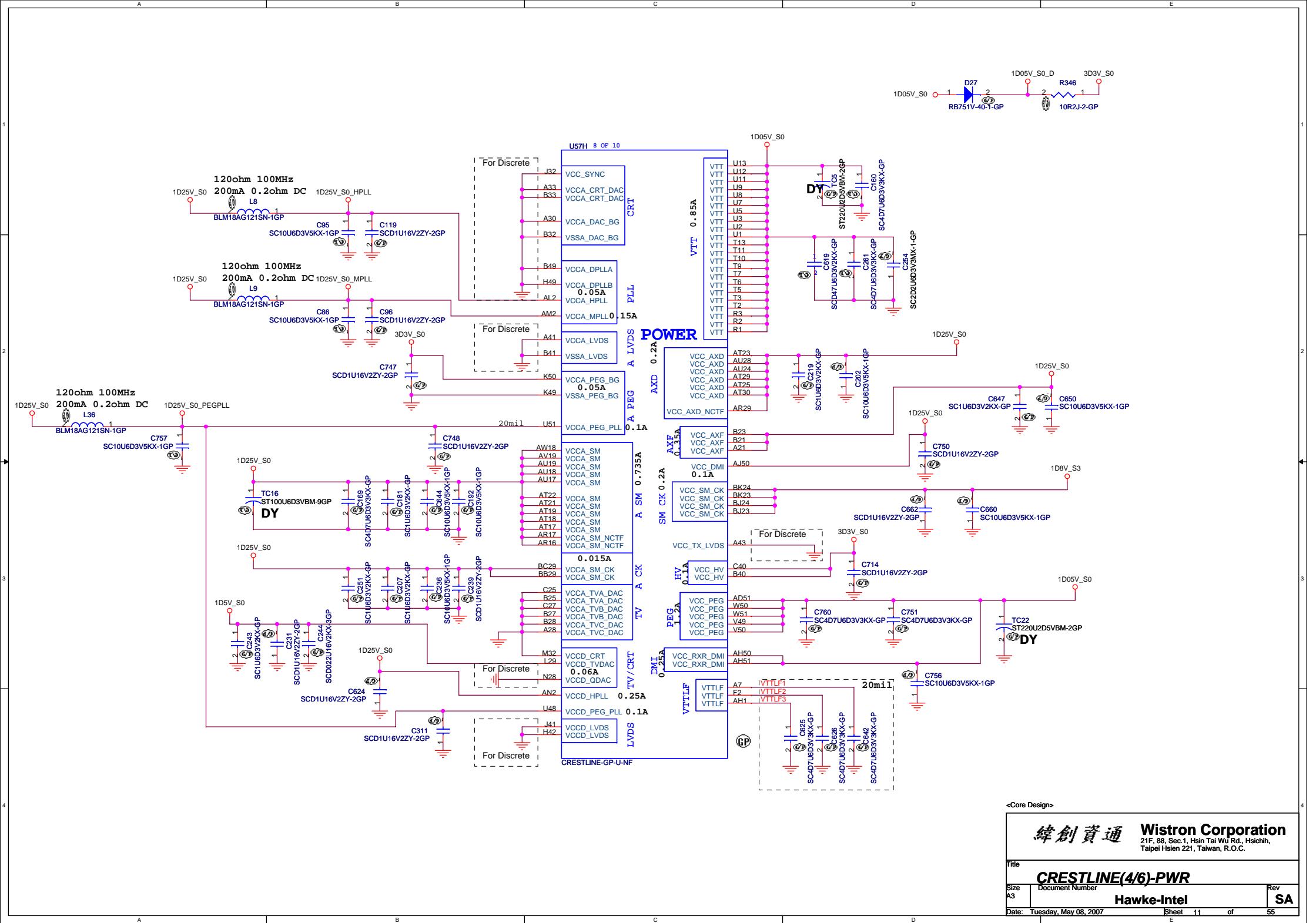
CRESTLINE-GP-U-NF

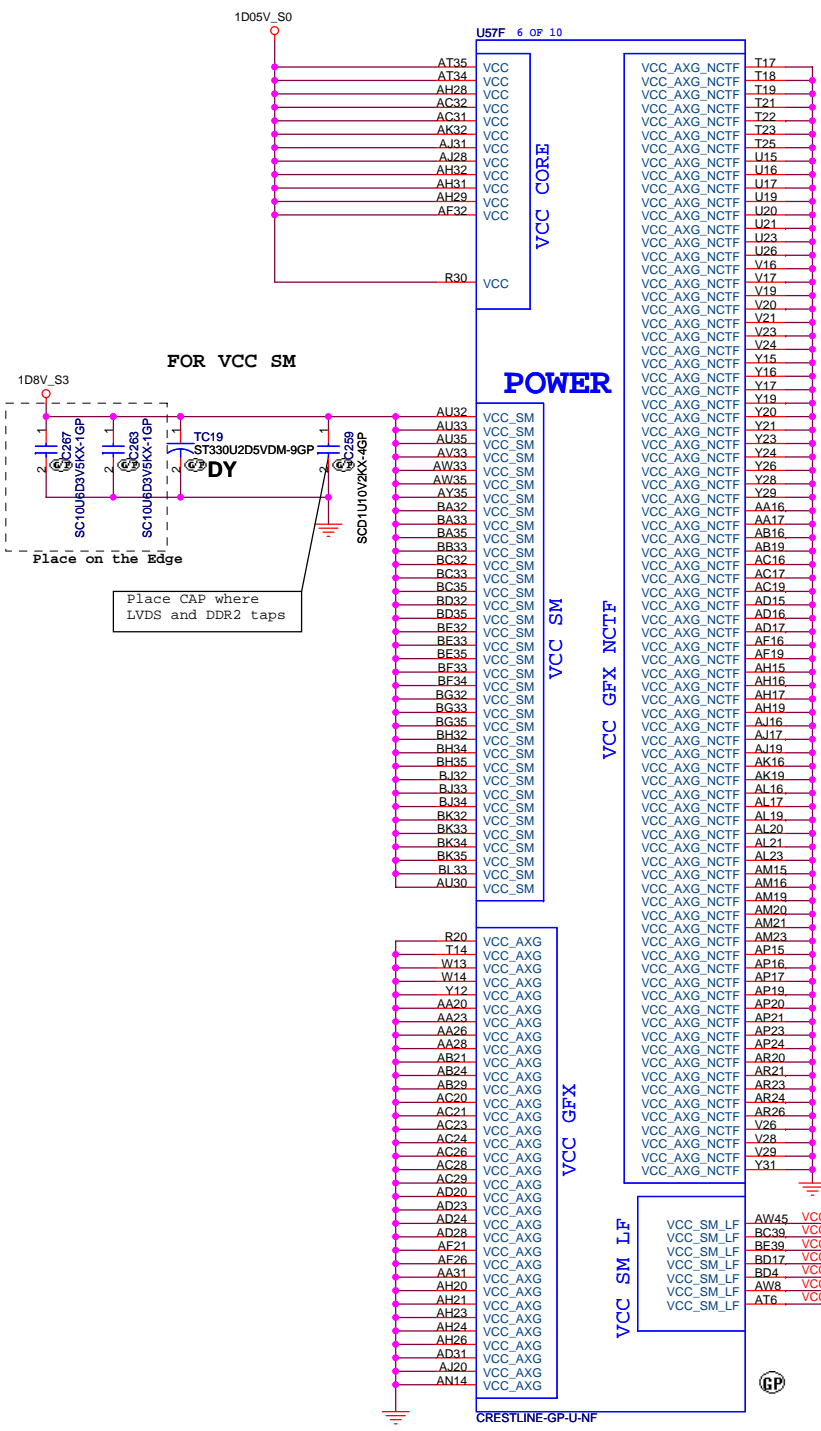


<Core Design>

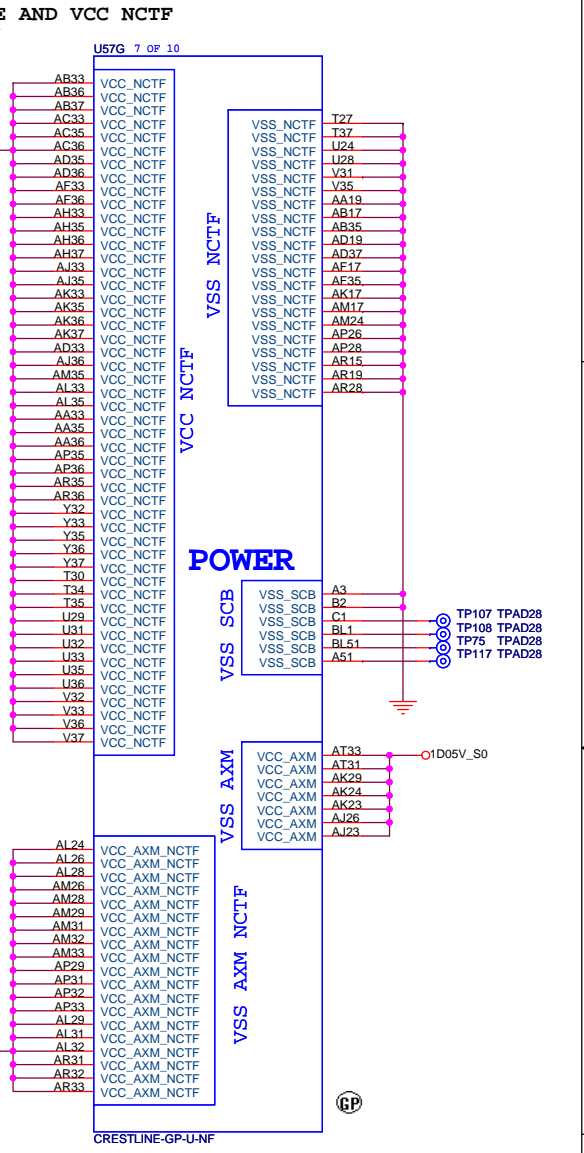
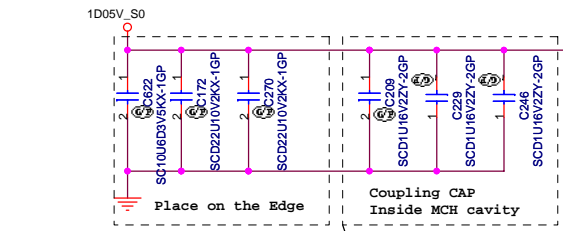
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
CRESTLINE(2/6)-DDR2 A/B CH
Size A3 Document Number
Date: Tuesday, May 08, 2007 Sheet 9 of 55
Hawke-Intel
Rev SA





Supply	Signal Group	Icc-max
+1.05V_VCCP	VCC	1.31A
+1.05V_VCCP	VCC_NCTF	A
+1.05V_VCCP	VT	0.85A
+1.05V_VCCP	VCC_PEG	1.2A
+1.05V_VCCP	VCC_RXR_DMI	0.25A
+1.05V_VCCP	VCC_ATX	84.15mA
+1.8V_SUS	VCC_SM	2.4A
+1.8V_SUS	VCC_SM_CK	0.2A
+1.25V_RUN	VCCA_HPLL	0.05A
+1.25V_RUN	VCCA_MPLL	0.15A
+1.25V_RUN	VCCA_SM	0.735A
+1.25V_RUN	VCCA_SM_NCTF	A
+1.25V_RUN	VCCA_SM_CK	0.015A
+1.25V_RUN	VCCD_HPLL	0.25A
+1.25V_RUN	VCCA_AXD	0.2A
+1.25V_RUN	VCCA_AXD_NCTF	A
+1.25V_RUN	VCCA_PEG_PLL	0.1A
+1.25V_RUN	VCCA_AXF	0.35A
+1.25V_RUN	VCCA_DMI	0.1A
+1.5V_RUN	VCCD_TV DAC	0.06A
+3.3V_RUN	VCCA_PEG_BG	0.005A
+3.3V_RUN	VCC_HV	0.1A



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A13	VSS	VSS	AW24
A15	VSS	VSS	AW29
A17	VSS	VSS	AW32
A24	VSS	VSS	AW5
AA21	VSS	VSS	AW7
AA24	VSS	VSS	AY10
AA29	VSS	VSS	AY24
AB20	VSS	VSS	AY37
AB23	VSS	VSS	AY42
AB26	VSS	VSS	AY43
AB28	VSS	VSS	AY45
AB31	VSS	VSS	AY47
AC10	VSS	VSS	AY50
AC13	VSS	VSS	B10
AC3	VSS	VSS	B20
AC39	VSS	VSS	B24
AC43	VSS	VSS	B29
AD1	VSS	VSS	B30
AD21	VSS	VSS	B35
AD26	VSS	VSS	B38
AD29	VSS	VSS	B43
AD3	VSS	VSS	B46
AD41	VSS	VSS	B5
AD45	VSS	VSS	B8
AD49	VSS	VSS	BA1
AD5	VSS	VSS	BA17
AD50	VSS	VSS	BA18
AD8	VSS	VSS	BA2
AE10	VSS	VSS	BA24
AE14	VSS	VSS	BB12
AE6	VSS	VSS	BB25
AF20	VSS	VSS	BB40
AF23	VSS	VSS	BB44
AF24	VSS	VSS	BB49
AF31	VSS	VSS	BB8
AG2	VSS	VSS	BC16
AG38	VSS	VSS	BC24
AG43	VSS	VSS	BC25
AG47	VSS	VSS	BC36
AG50	VSS	VSS	BC40
AH3	VSS	VSS	BC51
AH40	VSS	VSS	BD13
AH41	VSS	VSS	BD2
AH7	VSS	VSS	BD28
AH9	VSS	VSS	BD45
AJ11	VSS	VSS	BD48
AJ13	VSS	VSS	BD5
AJ21	VSS	VSS	BE1
AJ24	VSS	VSS	BE19
AJ29	VSS	VSS	BE23
AJ32	VSS	VSS	BE30
AJ43	VSS	VSS	BE42
AJ45	VSS	VSS	BE51
AJ49	VSS	VSS	BE8
AK20	VSS	VSS	BF12
AK21	VSS	VSS	BF16
AK26	VSS	VSS	BF36
AK28	VSS	VSS	BG19
AK31	VSS	VSS	BG2
AK51	VSS	VSS	BG24
AL1	VSS	VSS	BG29
AM11	VSS	VSS	BG39
AM13	VSS	VSS	BG48
AM3	VSS	VSS	BG5
AM4	VSS	VSS	BG51
AM41	VSS	VSS	BH17
AM45	VSS	VSS	BH30
AN1	VSS	VSS	BH44
AN38	VSS	VSS	BH46
AN39	VSS	VSS	BH8
AN43	VSS	VSS	BJ11
AN5	VSS	VSS	BJ13
AN7	VSS	VSS	BJ38
AP4	VSS	VSS	BJ4
AP48	VSS	VSS	BJ42
AP50	VSS	VSS	BJ46
AR11	VSS	VSS	BK12
AR2	VSS	VSS	BK17
AR39	VSS	VSS	BK25
AR44	VSS	VSS	BK29
AR47	VSS	VSS	BK36
AR7	VSS	VSS	BK40
AT10	VSS	VSS	BK44
AT14	VSS	VSS	BK6
AT41	VSS	VSS	BK8
AT49	VSS	VSS	BL11
AU1	VSS	VSS	BL13
AU23	VSS	VSS	BL19
AU29	VSS	VSS	BL22
AU3	VSS	VSS	BL37
AU36	VSS	VSS	BL47
AU49	VSS	VSS	C12
AU51	VSS	VSS	C16
AV39	VSS	VSS	C19
AV48	VSS	VSS	C28
AW1	VSS	VSS	C29
AW12	VSS	VSS	C33
AW16	VSS	VSS	C36
			C41

CRESTLINE-GP-U-NF

U57J10 OF 10

C46	VSS	VSS	W11
C50	VSS	VSS	W39
C7	VSS	VSS	W43
D13	VSS	VSS	W47
D24	VSS	VSS	W5
D3	VSS	VSS	W7
D32	VSS	VSS	Y13
D39	VSS	VSS	Y2
D45	VSS	VSS	Y41
D49	VSS	VSS	Y45
E10	VSS	VSS	Y49
E16	VSS	VSS	Y5
E24	VSS	VSS	Y50
E28	VSS	VSS	Y11
E32	VSS	VSS	P29
E47	VSS	VSS	T29
F19	VSS	VSS	T31
F36	VSS	VSS	T33
F4	VSS	VSS	R28
F40	VSS		
F50	VSS		
G1	VSS		
G13	VSS		
G16	VSS	VSS	AA32
G19	VSS	VSS	AB32
G24	VSS	VSS	AD32
G28	VSS	VSS	AF28
G29	VSS	VSS	AF29
G33	VSS	VSS	AT27
G42	VSS	VSS	AV25
G45	VSS	VSS	HS0
G48	VSS		
G8	VSS		
H24	VSS		
H28	VSS		
H4	VSS		
H45	VSS		
J11	VSS		
J16	VSS		
J2	VSS		
J24	VSS		
J28	VSS		
J33	VSS		
J35	VSS		
J39	VSS		
K12	VSS		
K47	VSS		
K8	VSS		
L1	VSS		
L17	VSS		
L20	VSS		
L24	VSS		
L28	VSS		
L3	VSS		
L33	VSS		
L49	VSS		
M28	VSS		
M42	VSS		
M46	VSS		
M49	VSS		
M5	VSS		
M50	VSS		
M9	VSS		
N11	VSS		
N14	VSS		
N17	VSS		
N29	VSS		
N32	VSS		
N36	VSS		
N39	VSS		
N44	VSS		
N49	VSS		
N7	VSS		
P19	VSS		
P2	VSS		
P23	VSS		
P3	VSS		
P50	VSS		
R49	VSS		
T39	VSS		
T43	VSS		
T47	VSS		
U41	VSS		
U45	VSS		
U50	VSS		
V2	VSS		
V3	VSS		

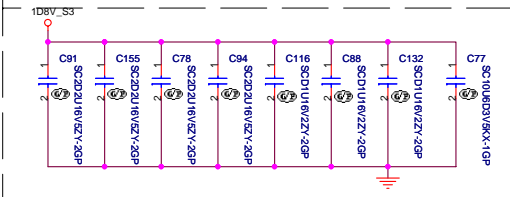
VSS

CRESTLINE-GP-U-NF

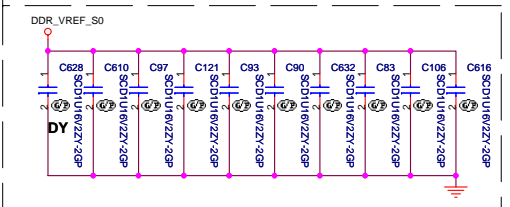
<Core Design>

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Title CRESTLINE(6/6)-PWR/GND		
Size A3	Document Number Hawke-Intel	Rev SA
Date: Tuesday, May 08, 2007	Sheet 13 of 55	

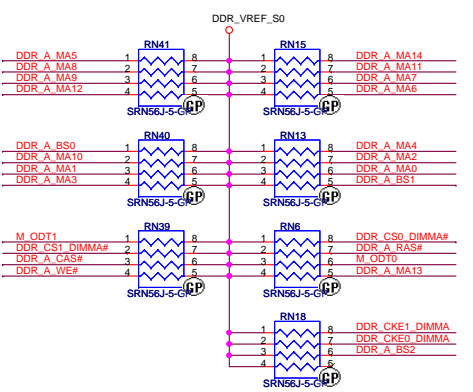
Layout Note:
Place near DM1



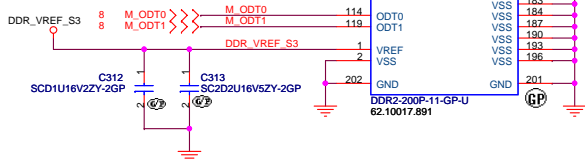
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

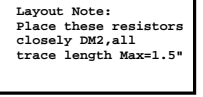
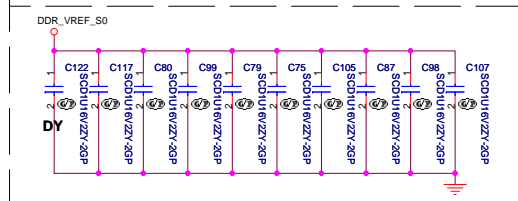


change to 8P4R

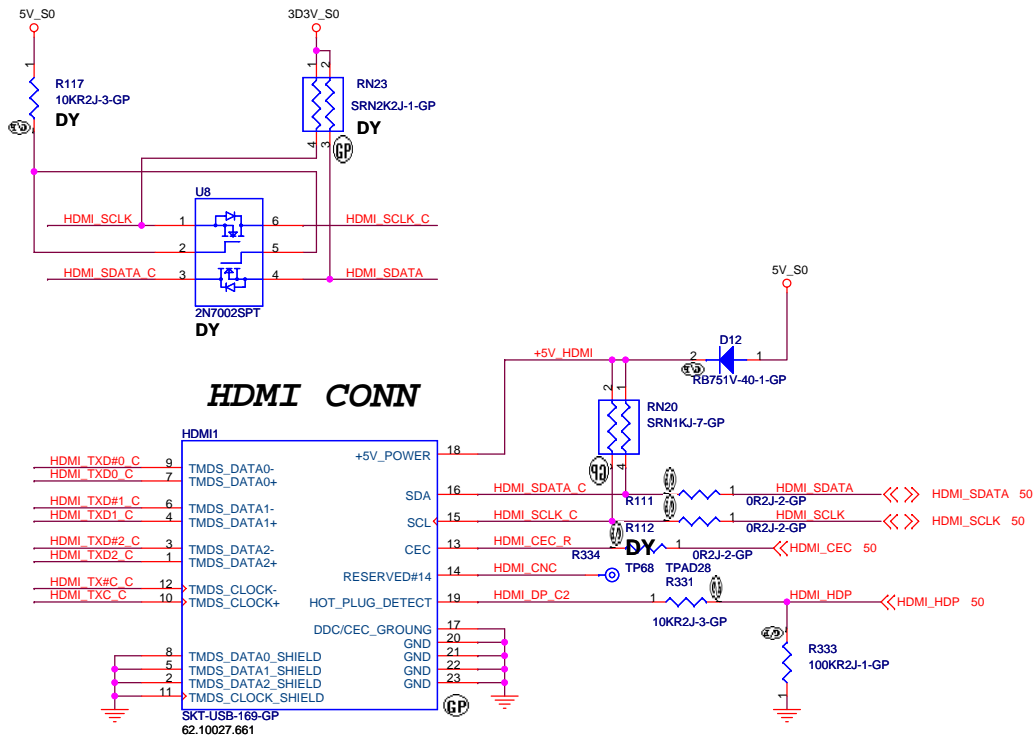
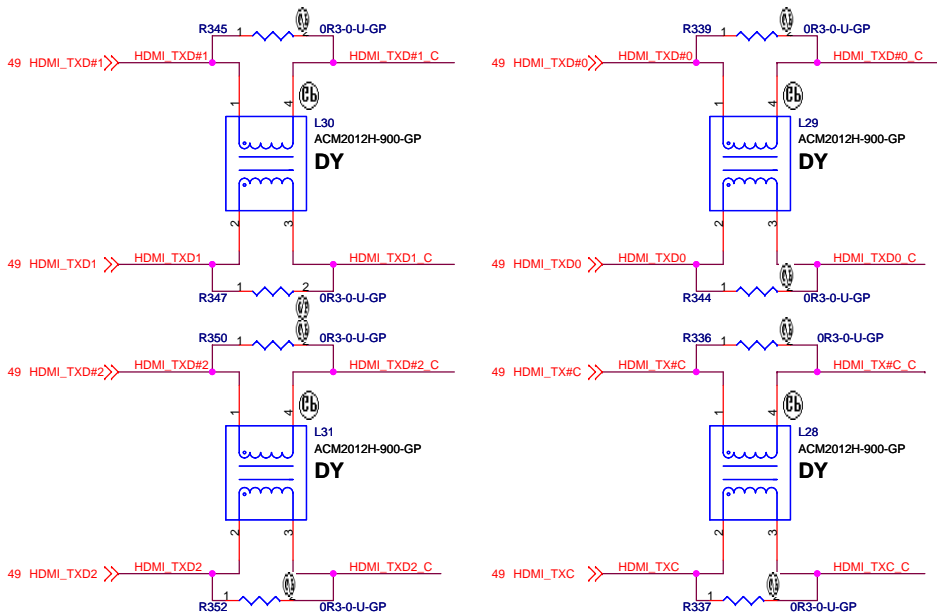


Layout Note:
Place these resistors closely DM1, all trace length Max=1.5"

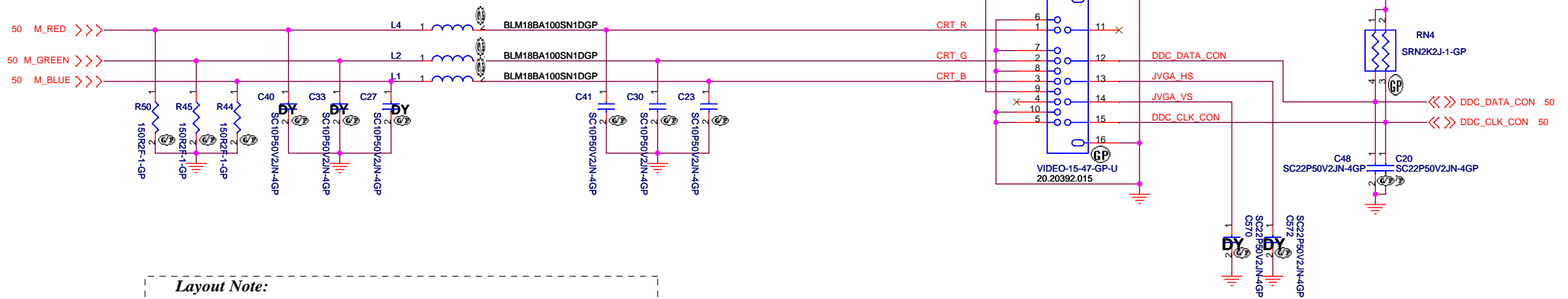




HDMI I/F & CONNECTOR

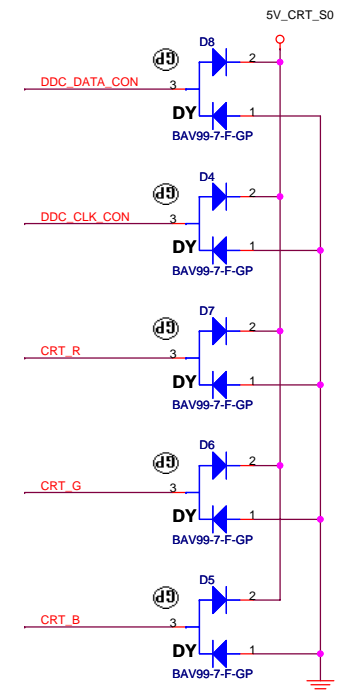
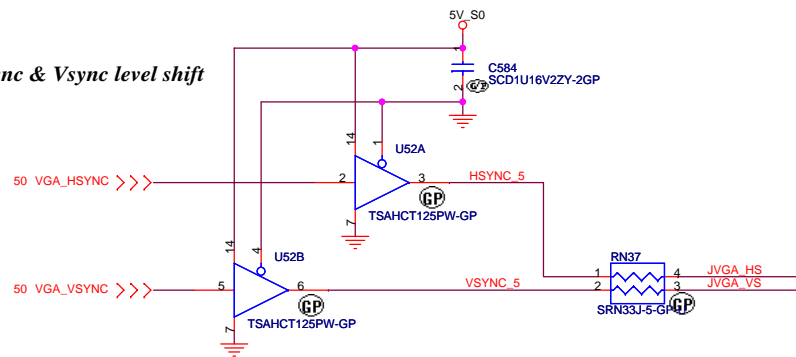


CRT I/F & CONNECTOR



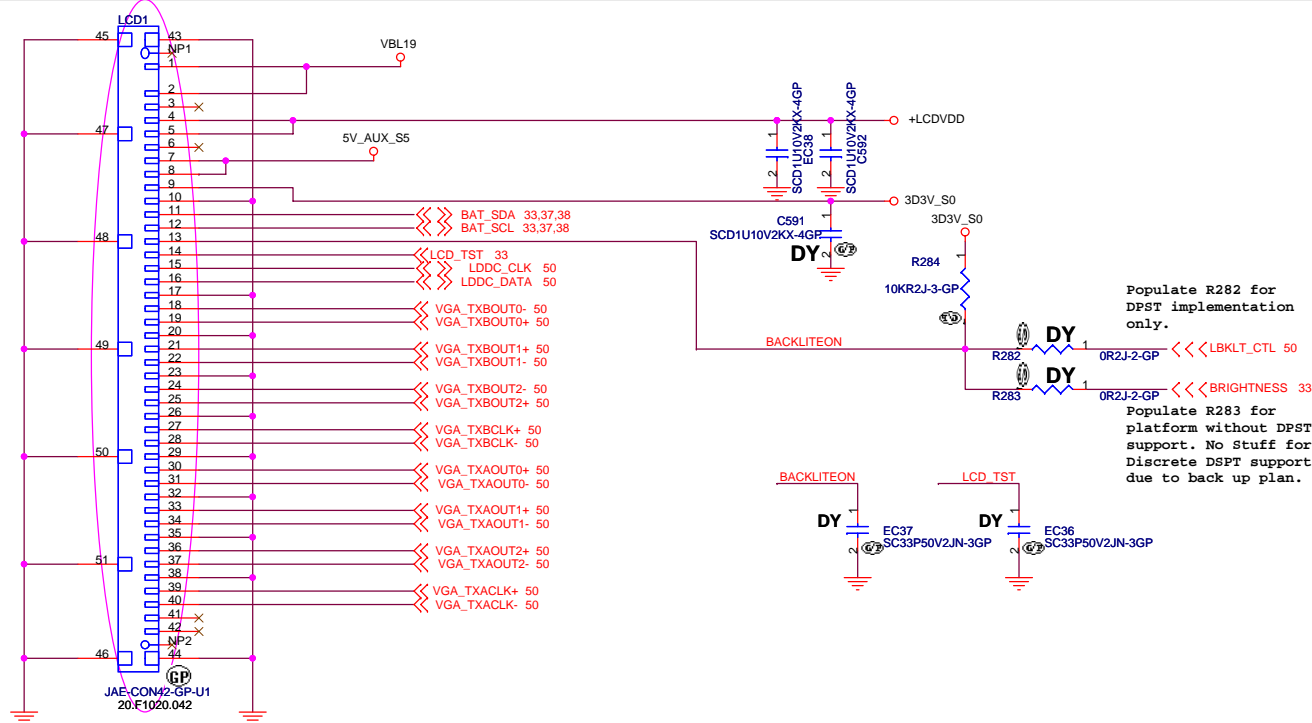
Layout Note:
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



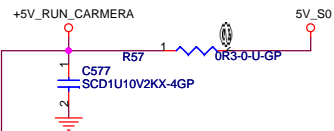
<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CRT Connector	
Size A3	Document Number
Date: Tuesday, May 08, 2007	Hawke-Intel Rev SA

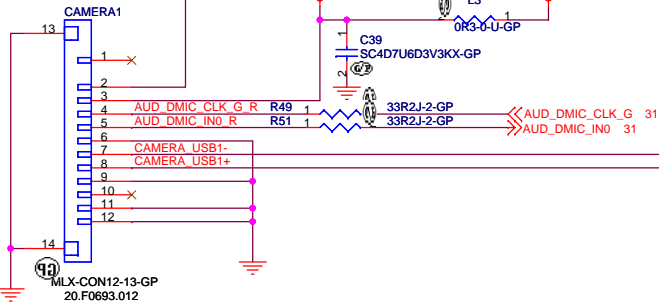
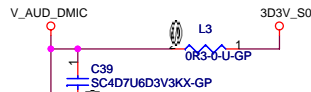


Will change to 40pin connector.
Need to add detect pin.
Wait for 40pin pin-definition.
20.F1093.040

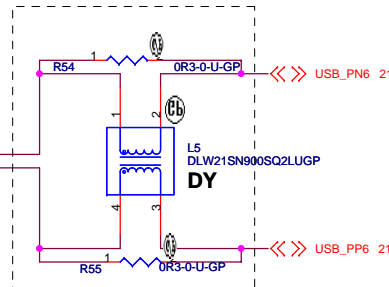
CAMERA Power



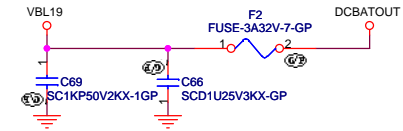
Mic Power



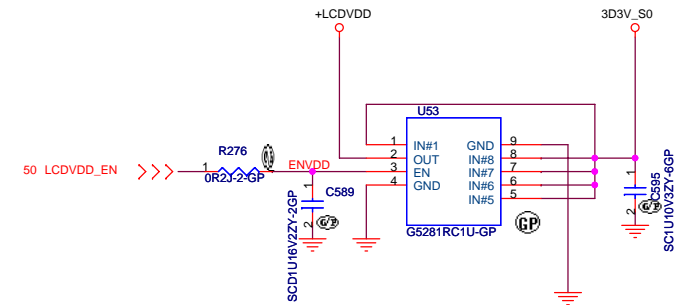
Place near connector CAMERA1.



INVERTER POWER



LCD POWER



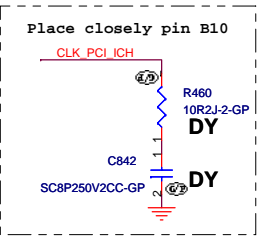
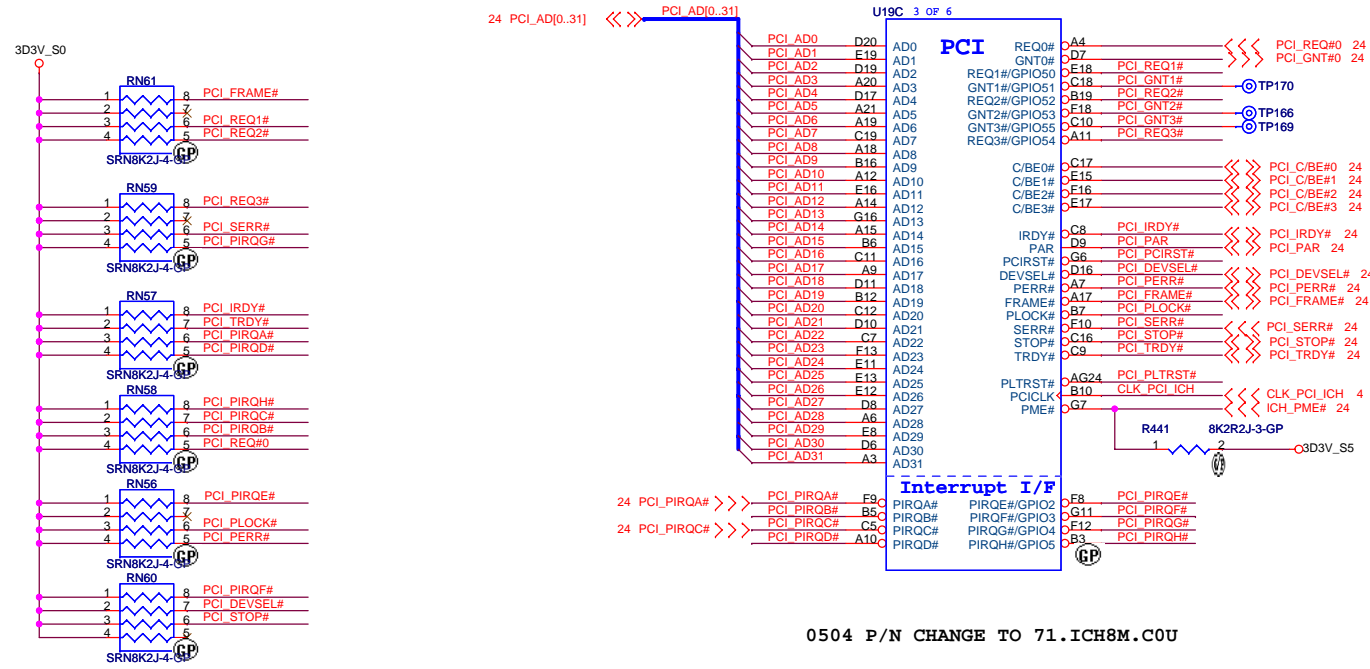
<Core Design>

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
LCD/Inverter/Camera		
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PCI Interface Routing

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD25	A D	0	0

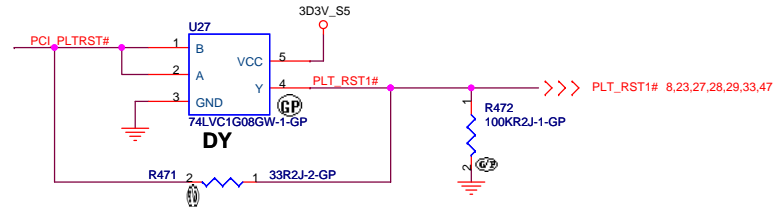
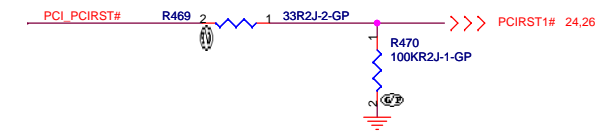
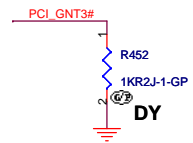


0504 P/N CHANGE TO 71.ICH8M.C0U

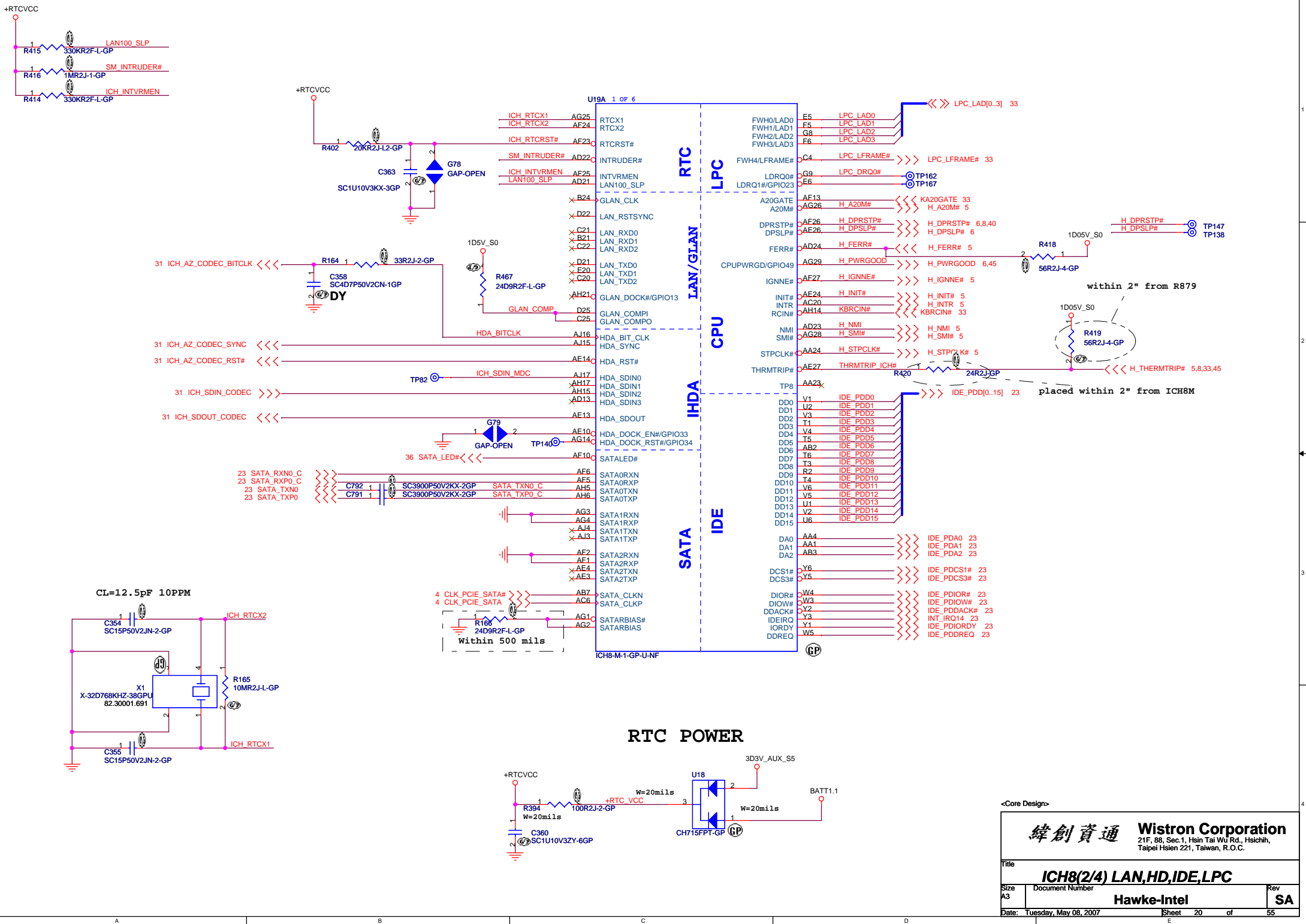
ICH8-Strap PIN

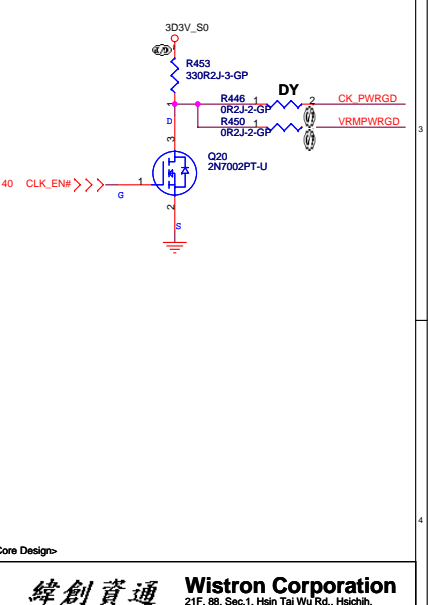
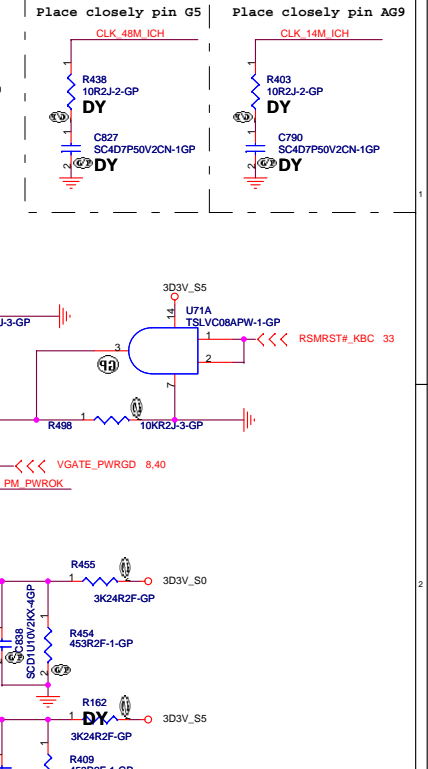
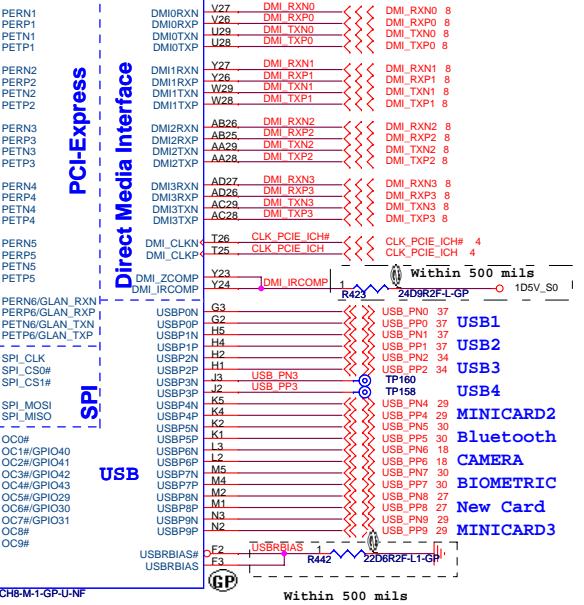
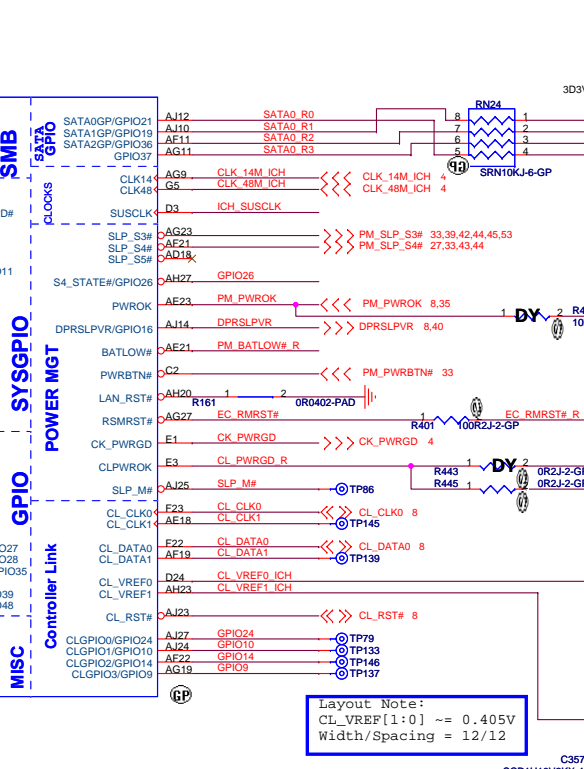
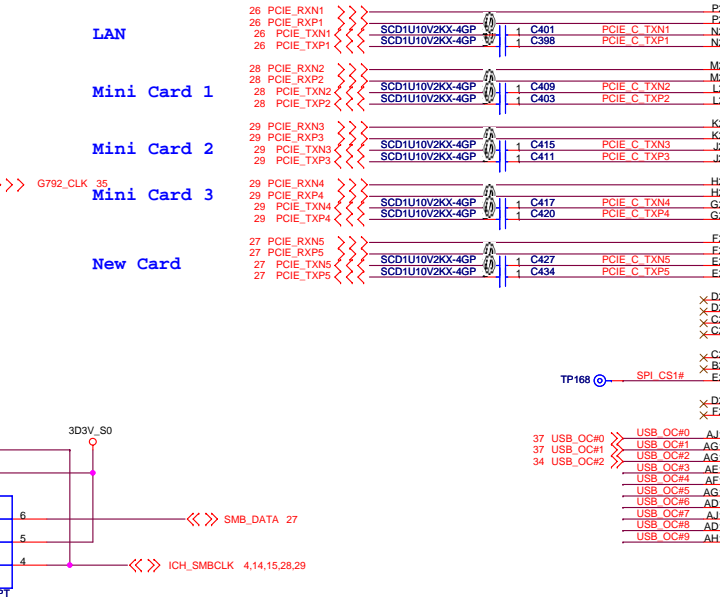
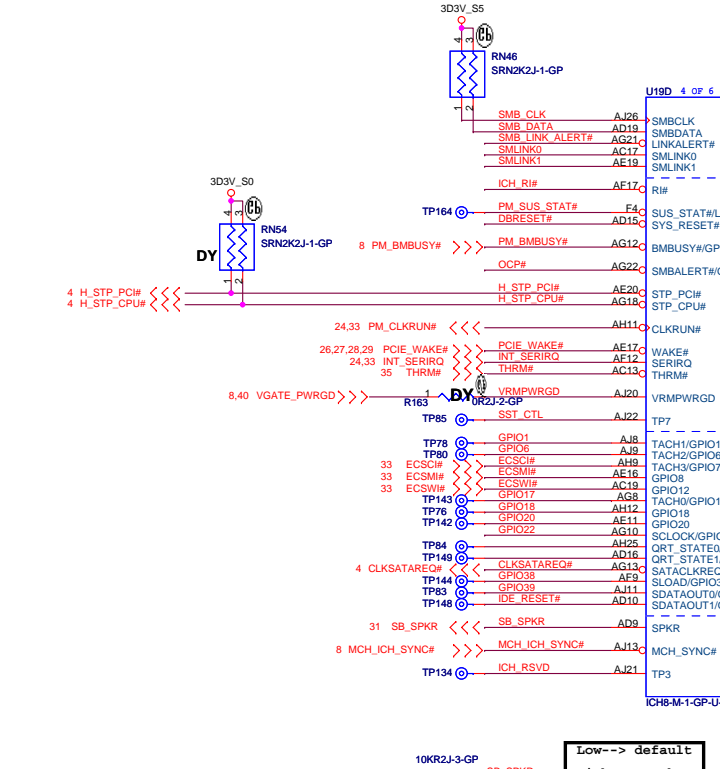
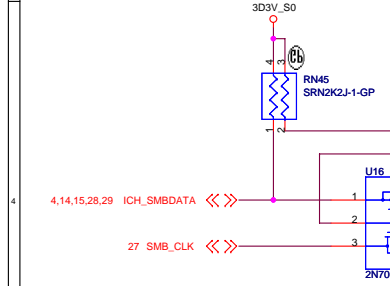
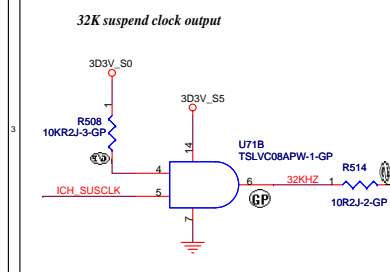
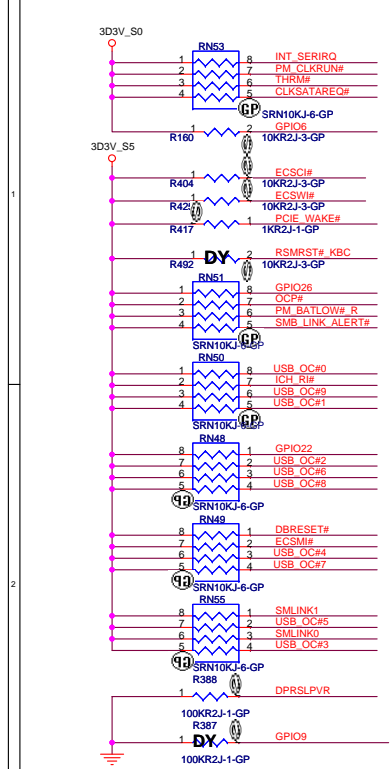
BOOT BIOS Strap		
PCI_GNT#0 (R166)	SPI_CS#1 (R167)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R168)	low = A16 swap override enable high = default	

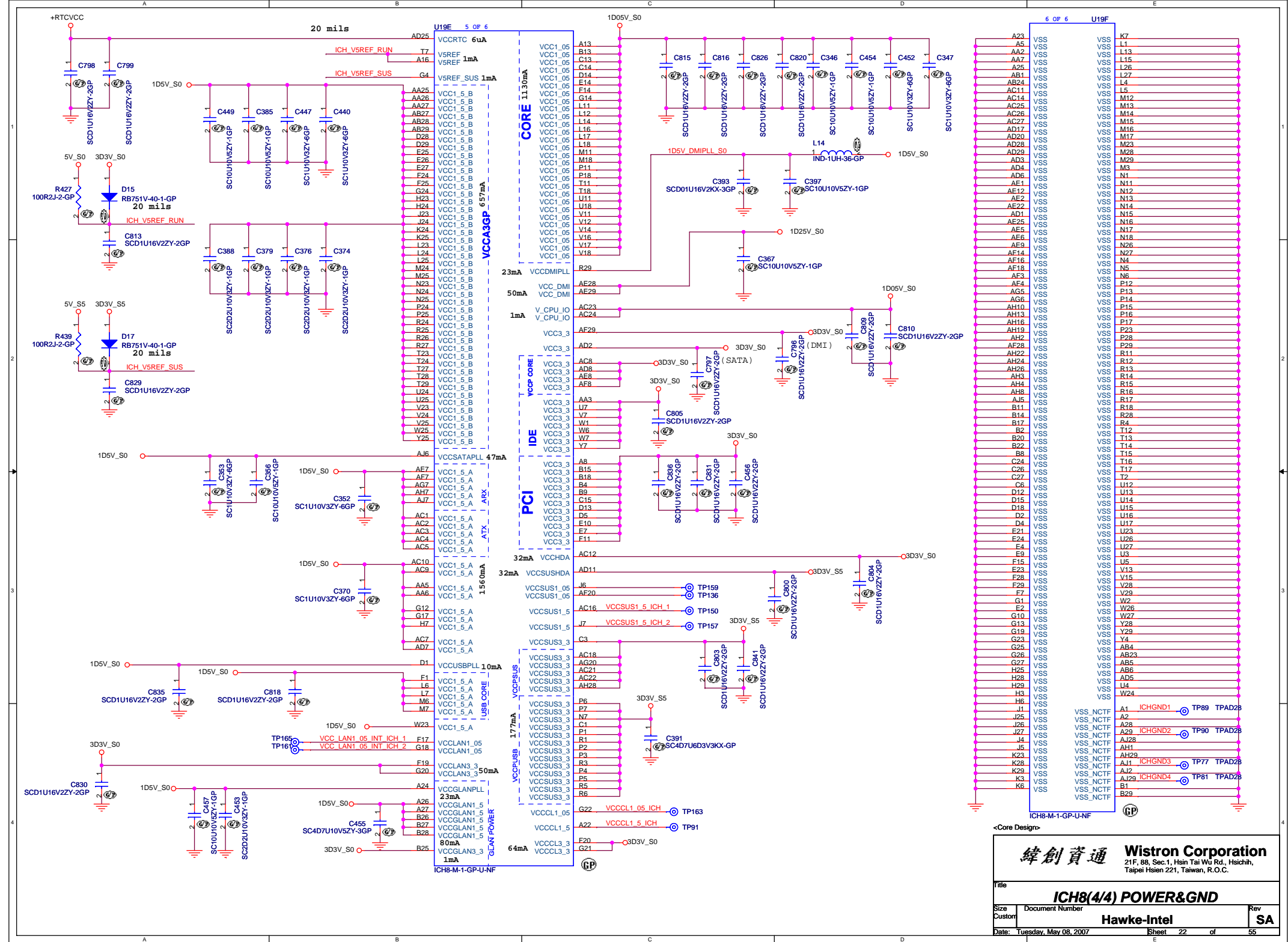
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



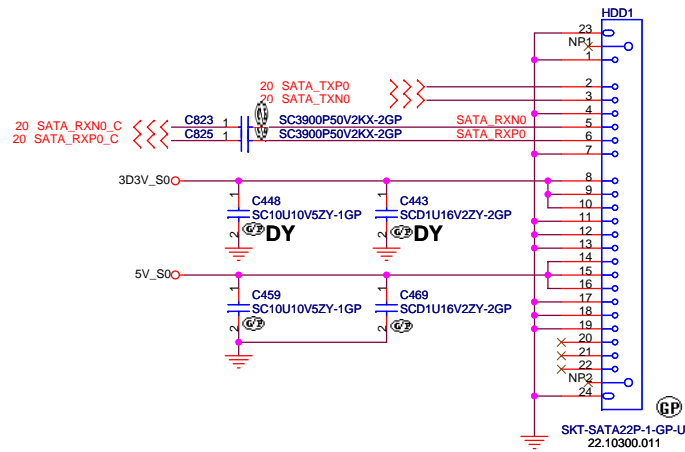
<Core Design>



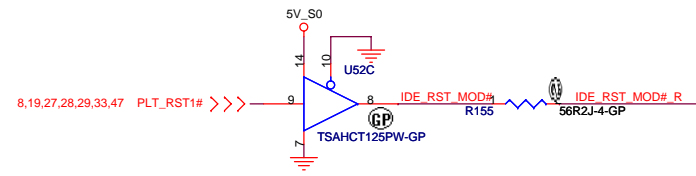
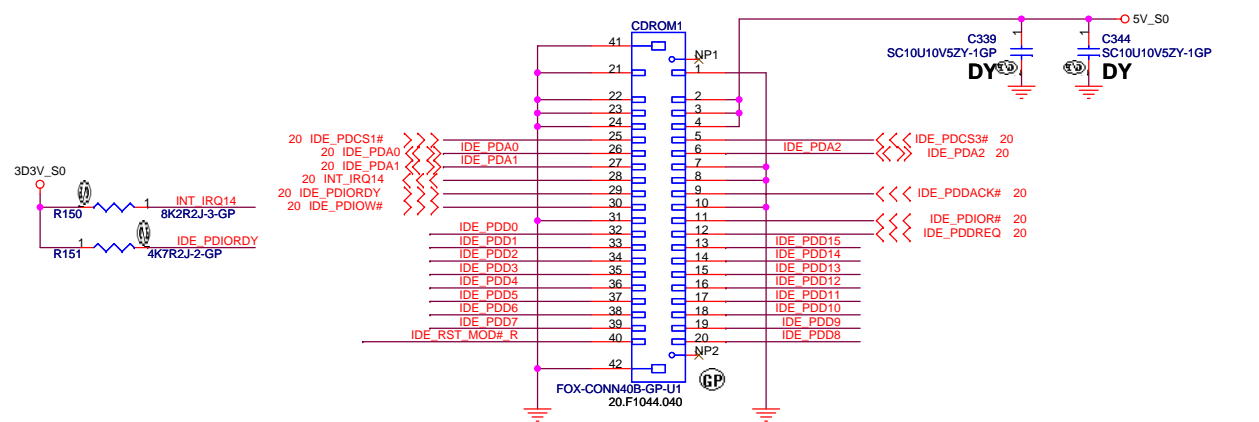


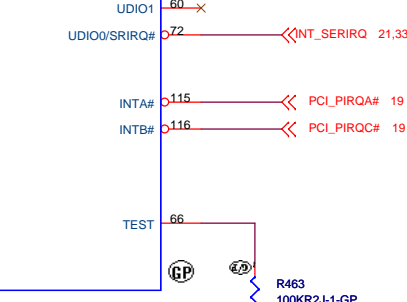
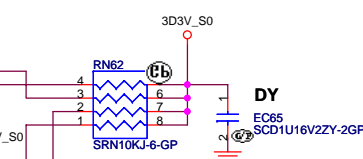
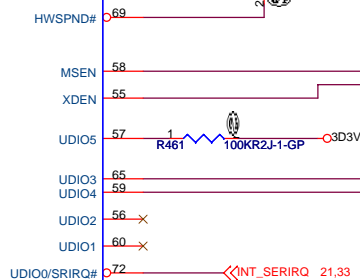


SATA HDD Connector

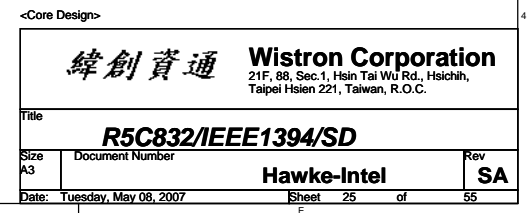


ODD Connector

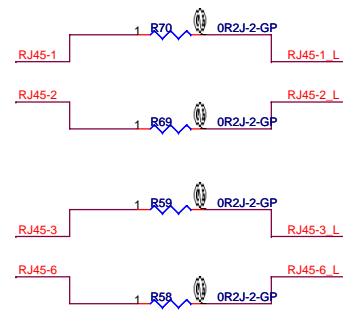
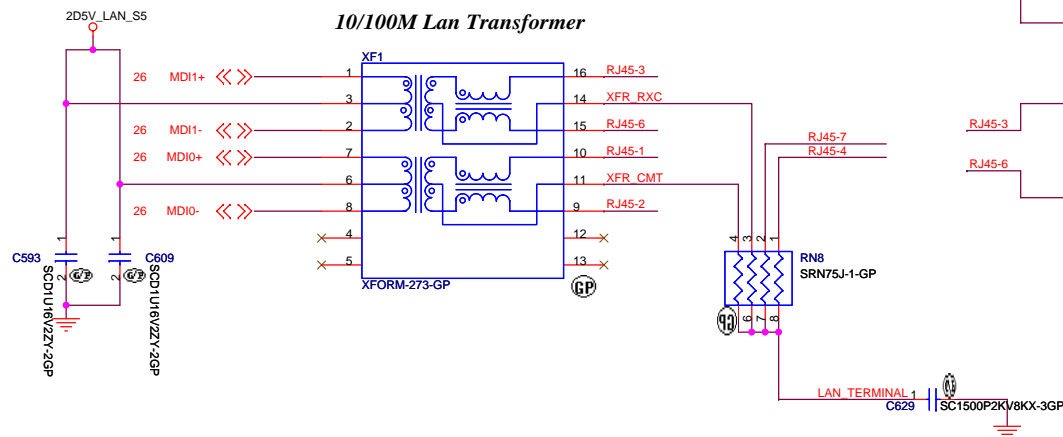




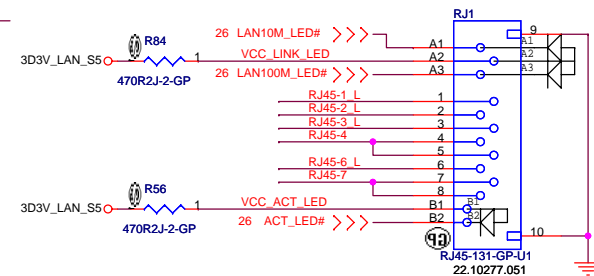
<Core Design>



RJ45 Connector



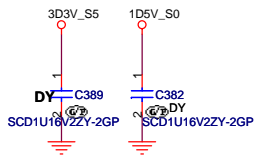
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.



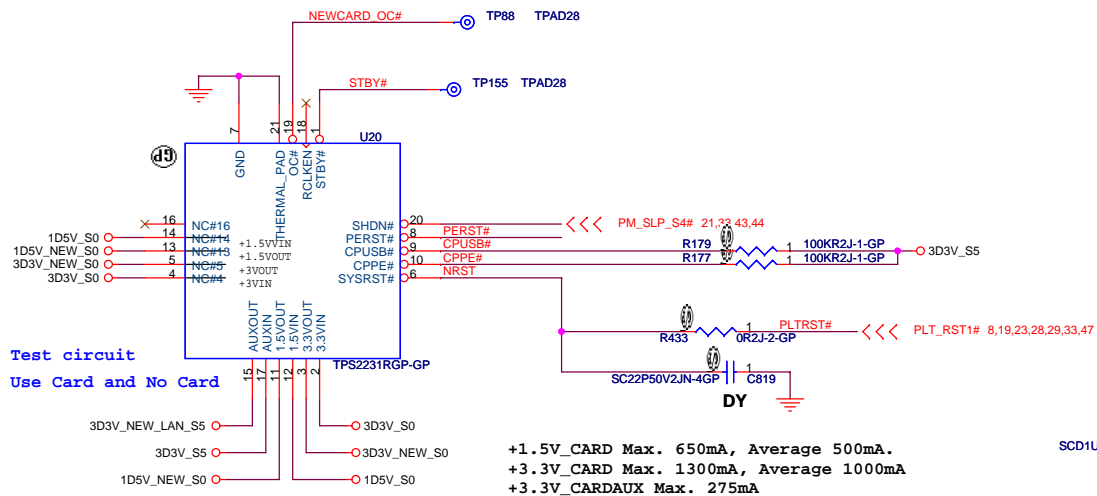
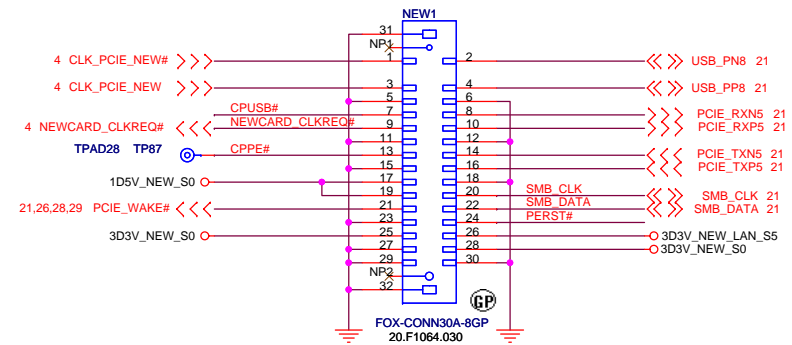
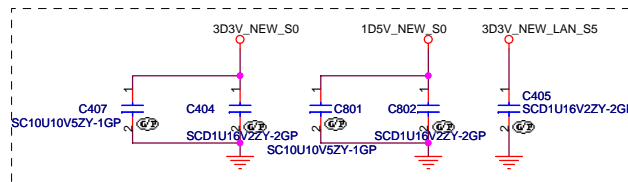
```
Yellow LED:TX/RX
Orange LED:Speed 100
Green LED:Speed 10
```

NEWCARD Connector

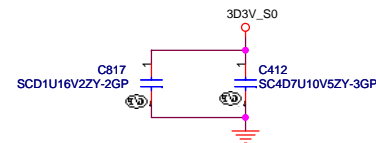
Place them Near to Chip



Place them Near to Connector



+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN connector/NEW CARD

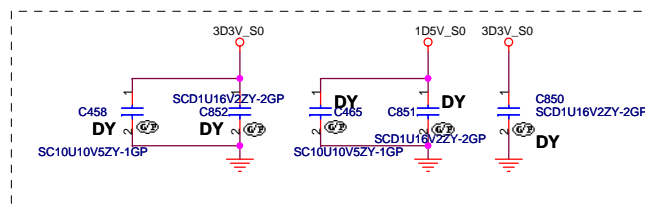
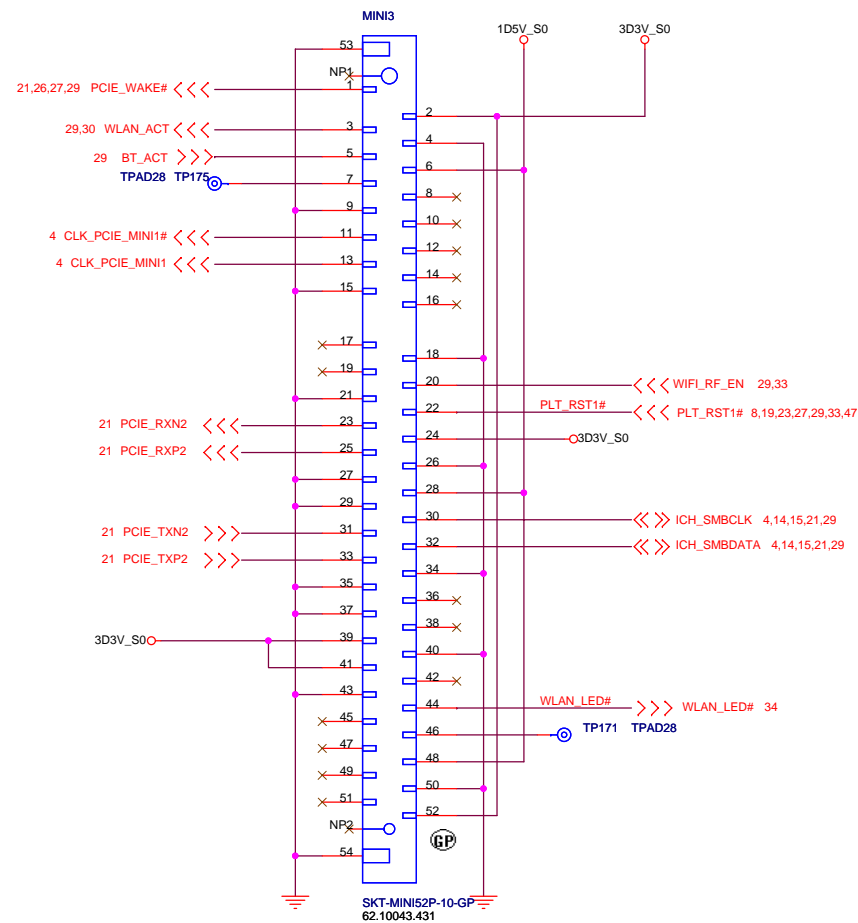
Size

Document Number

Hawke-Intel

Rev

Mini Card Connector 2(802.11a/b/g)



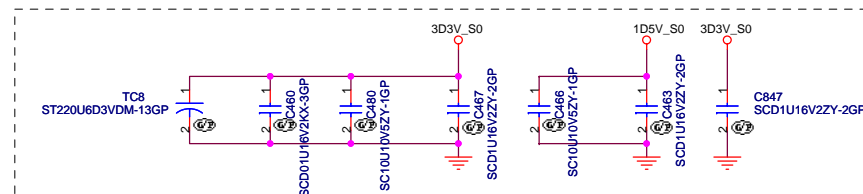
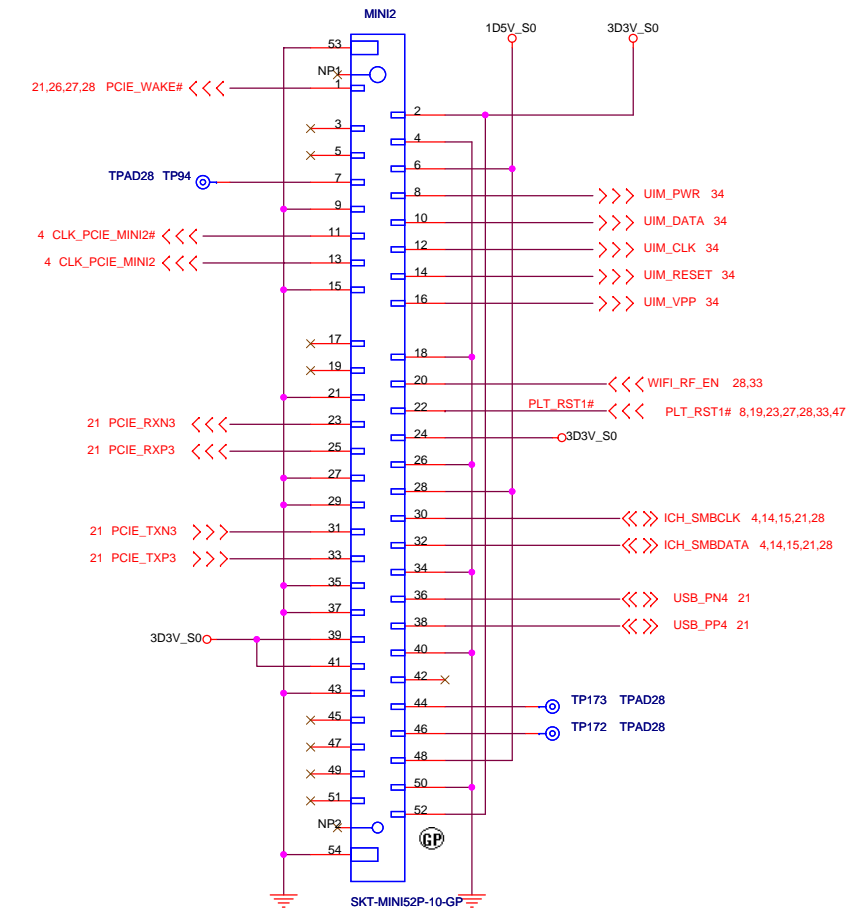
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

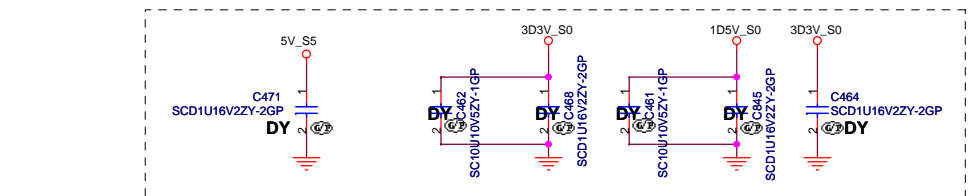
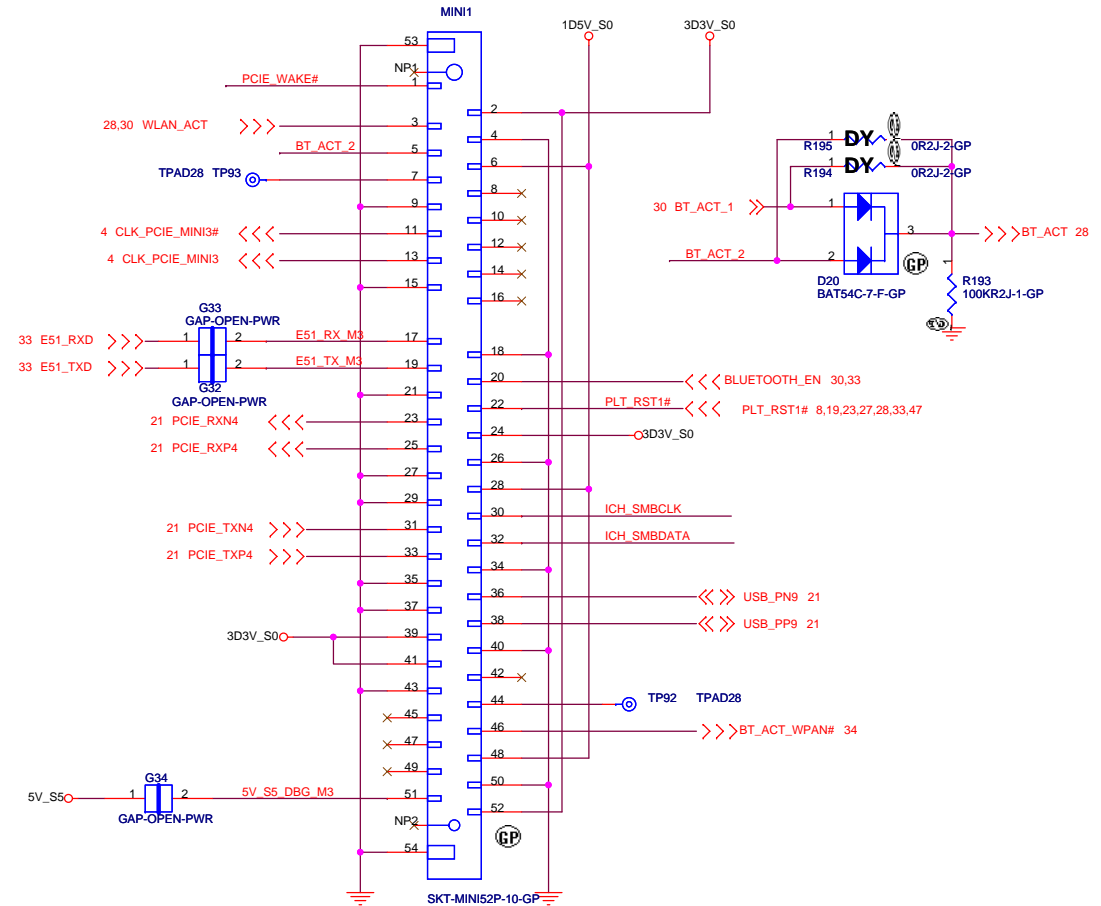
Title		
MINI CARD CONN 1		
Size	Document Number	Rev
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Mini Card Connector

Mini Card Connector 2(WWAN)



Mini Card Connector 3(Robson/BT)



<Core Design>

SPI FLASH ROM

SRN10KJ-6-GP
RN43

8M Bits

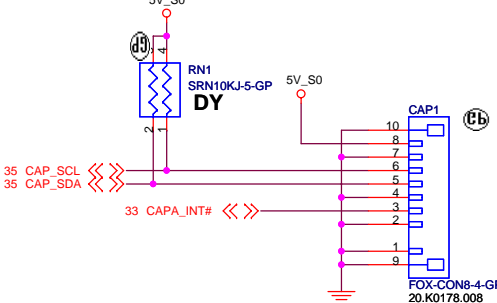
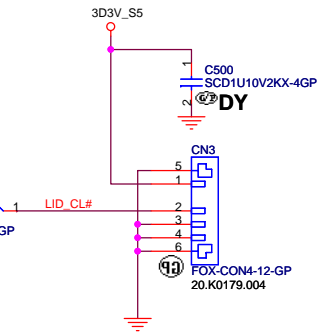
U61
W25X80-VSSI-GP

EMI REQUEST

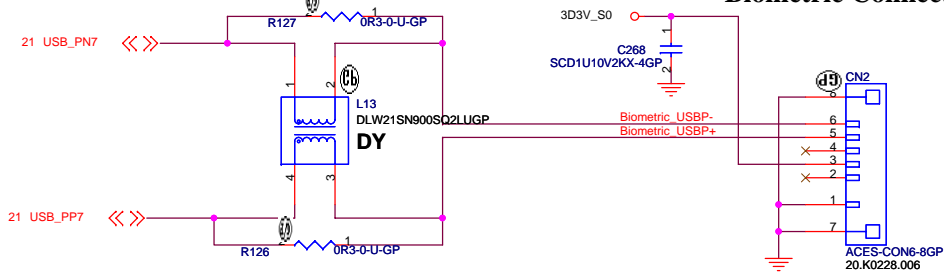
Place close to EC

To Hall Switch

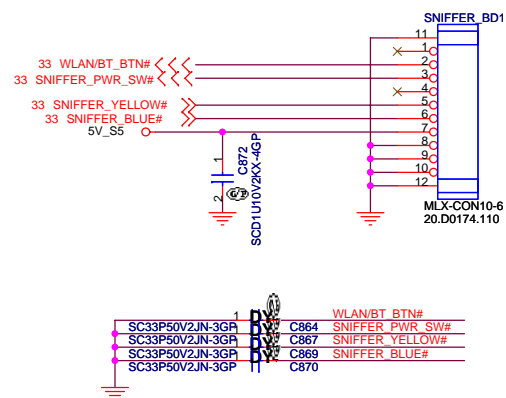
CAPACITY BUTTON



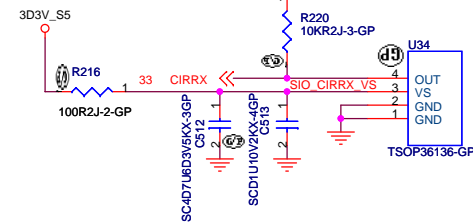
Biometric Connector



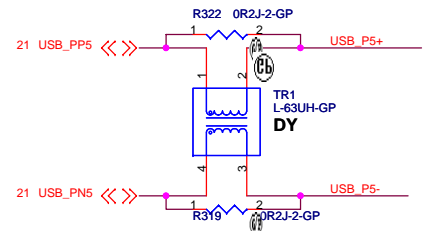
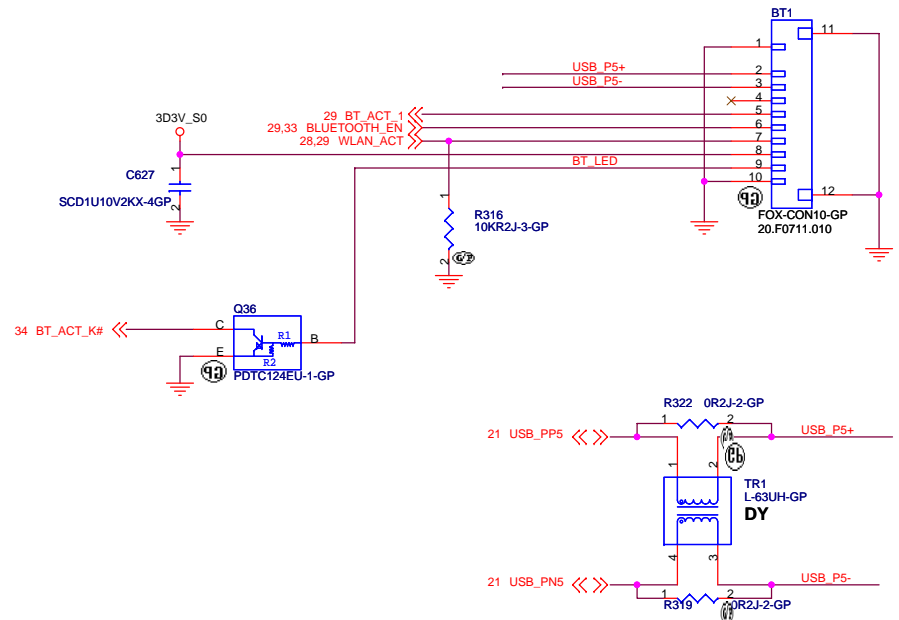
Switch Board

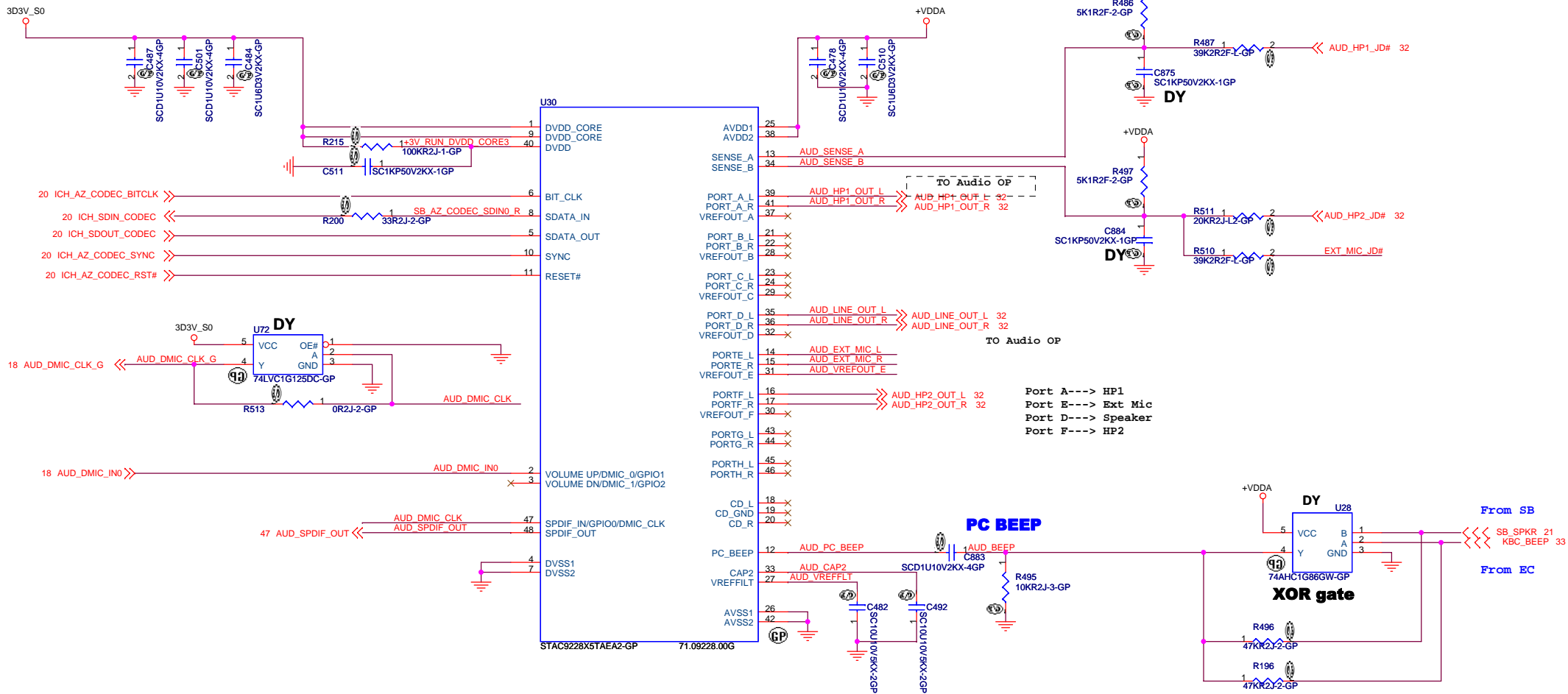


CIR

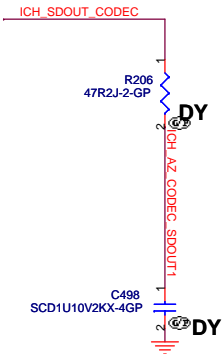


Bluetooth Module conn.





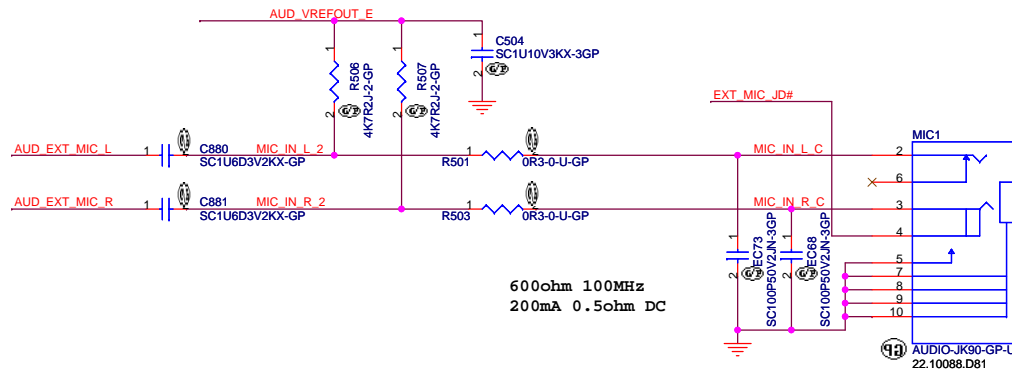
Azalia I/F EMI



Azalia I/F EMI

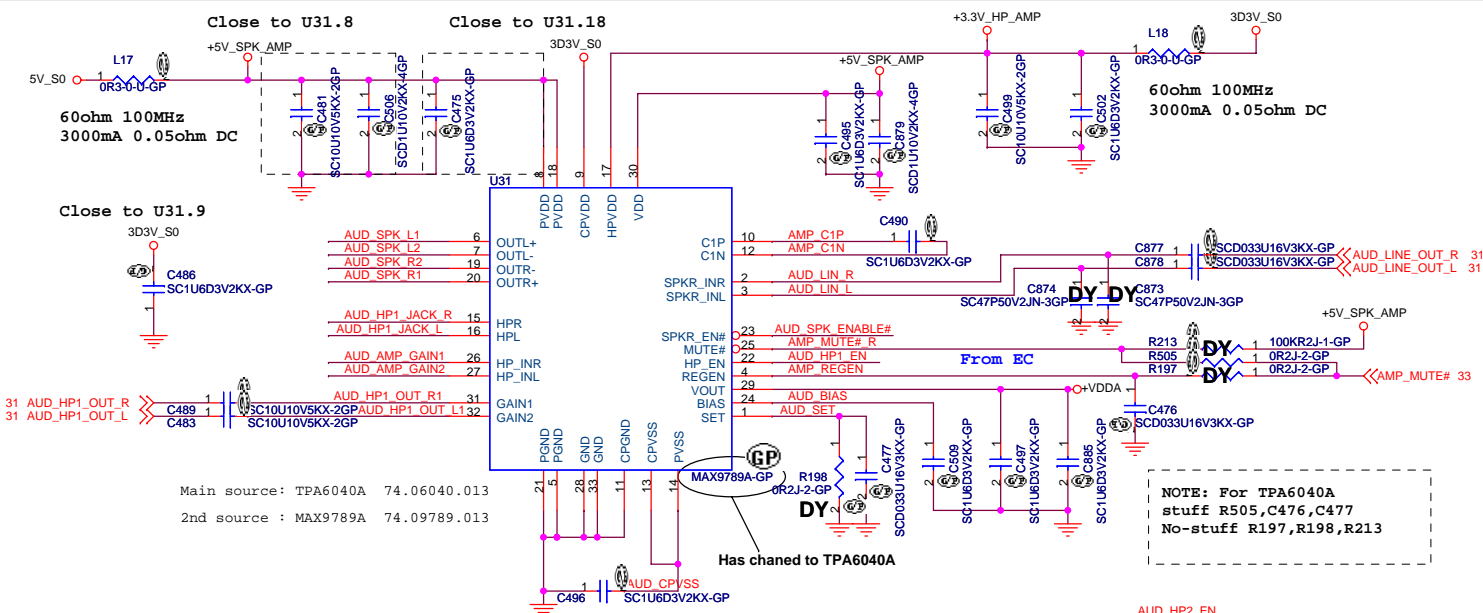


MIC IN

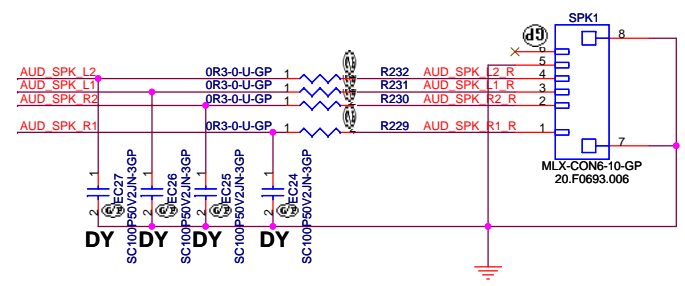


<Core Design>

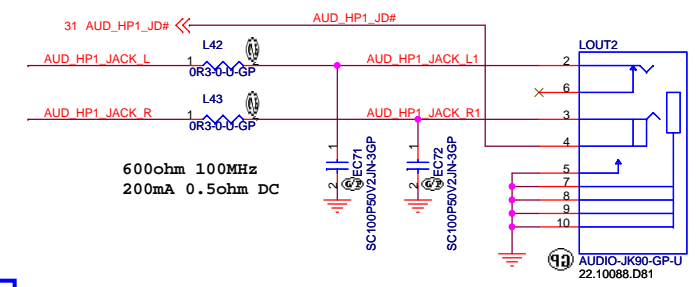
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
AUDIO CODEC STAC9228	
Size A3	Document Number
Hawke-Intel SA	
Date: Tuesday, May 08, 2007	Sheet 31 of 55



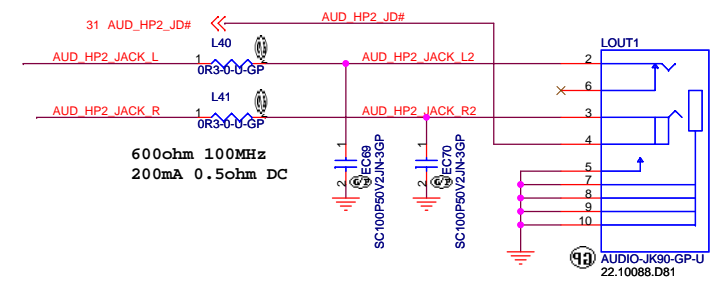
Speaker



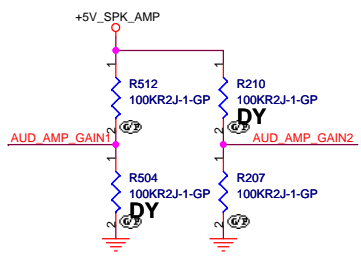
LINE1 OUT



LINE2 OUT

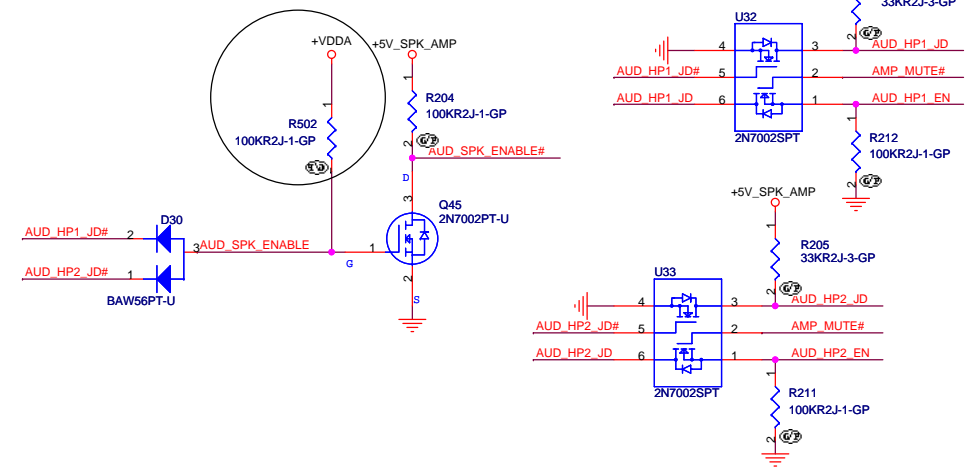


GAIN SETTING



GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown



WPC8763L STRAP PIN

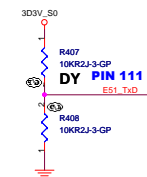
JENO (Pin 24)	JENK (Pin 53)	Functionality of Pins 17, 20, 21, 23 25, 27	Functionality of Pins 47, 48, 50, 51, 52
NO PD RES	GPIO Port	GPIO Port	Keyboard Scan
10K PD	NO PD	JTAG signals	Keyboard Scan
NO PD	10K PD	GPIO Port	JTAG signals

TRIS#(Pin 110) TRI-STATE

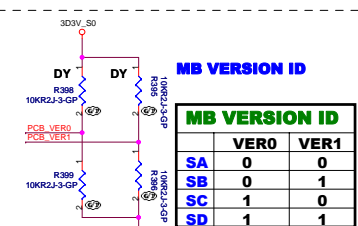
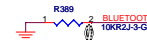
Forces the device to float all its output and I/O pins, if an external 10 KΩ pull-down resistor is connected.

BADDR1-0 (PIN 111, 112) I/O Base Address.

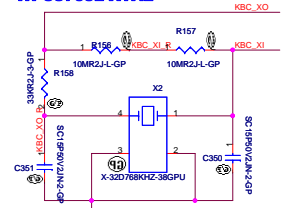
10KΩ external pull-down resistor on BADDR1: Core defined



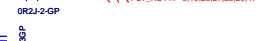
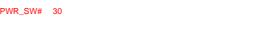
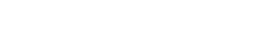
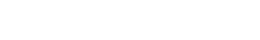
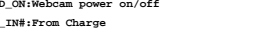
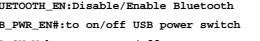
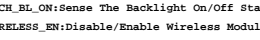
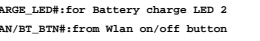
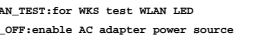
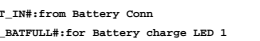
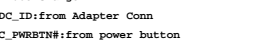
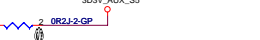
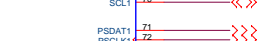
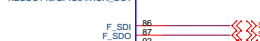
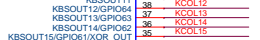
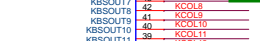
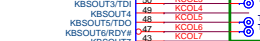
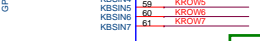
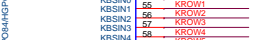
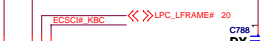
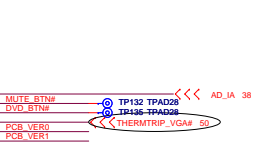
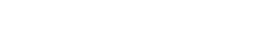
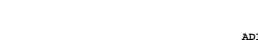
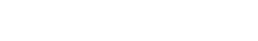
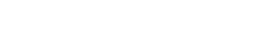
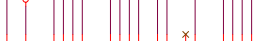
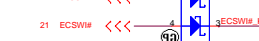
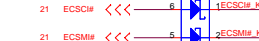
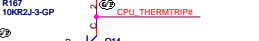
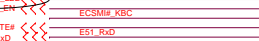
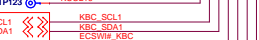
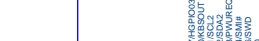
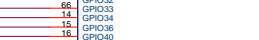
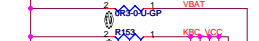
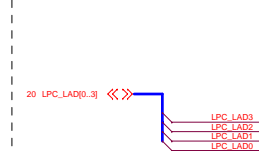
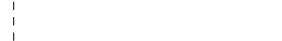
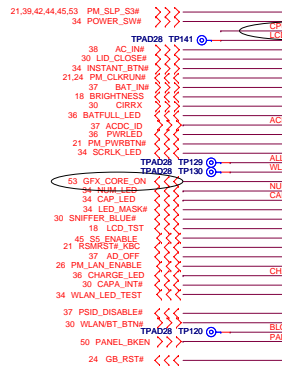
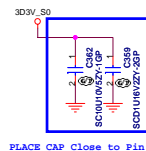
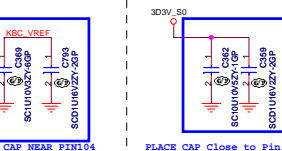
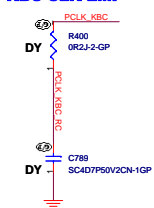
SHBM PIPN83 Shared Host BIOS Memory.
HIGH:NO SHARED(internal resistor)
LOW:SHARED BIOS memory.



WPC8763L XTAL

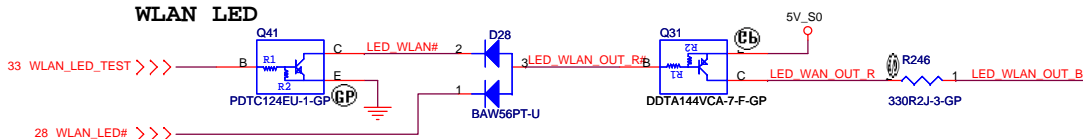


KBC CLK EMI

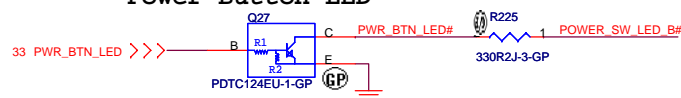




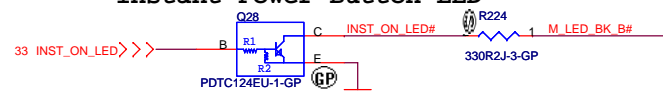
WLAN LED



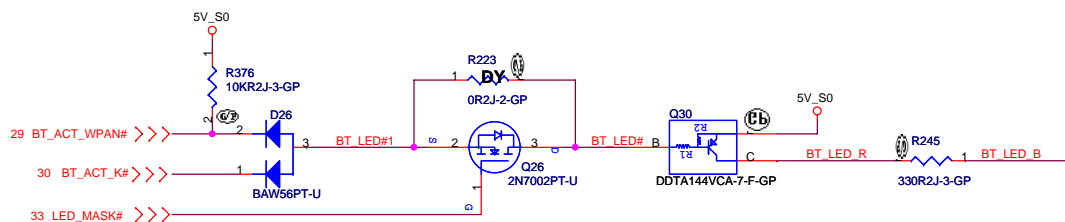
Power Button LED



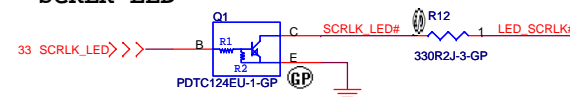
Instant Power Button LED



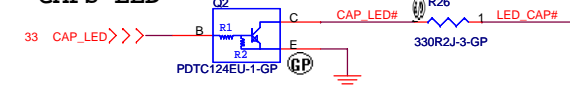
Bluetooth LED



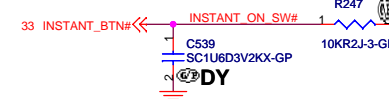
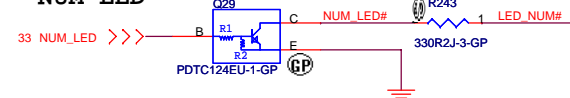
SCRLK LED



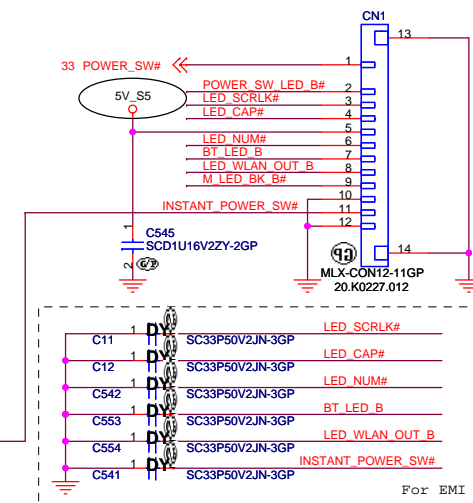
CAPS LED



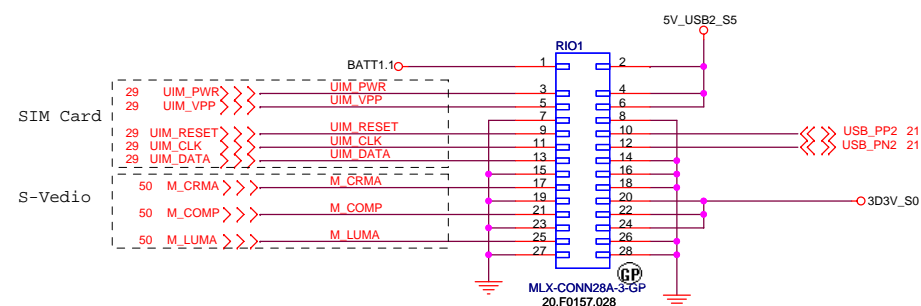
NUM LED



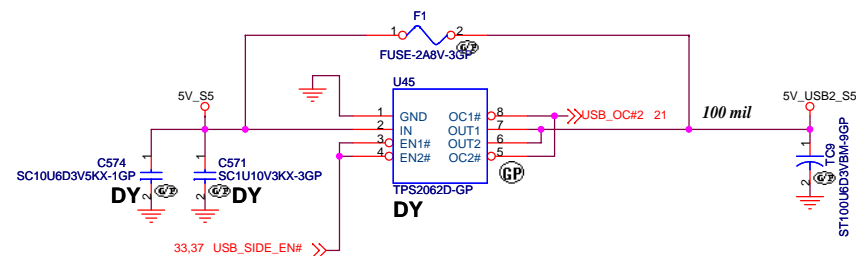
To LED Board



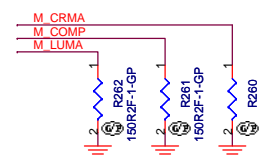
To Right I/O Board



USB POWER



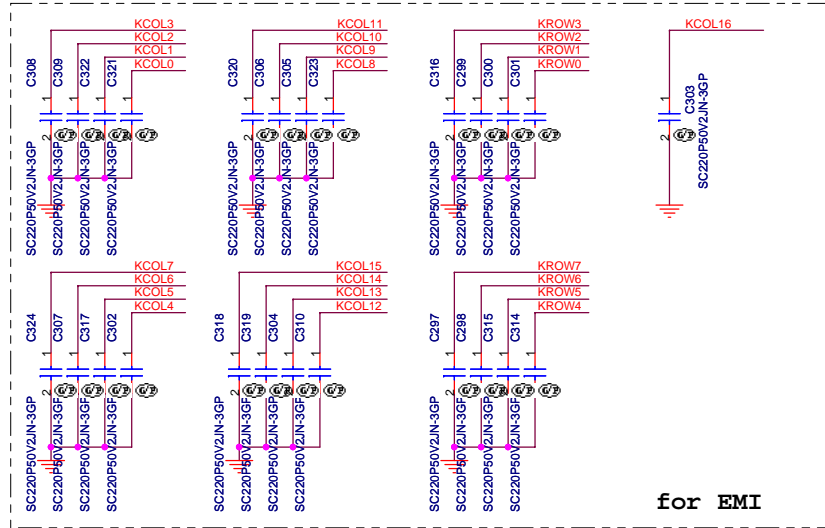
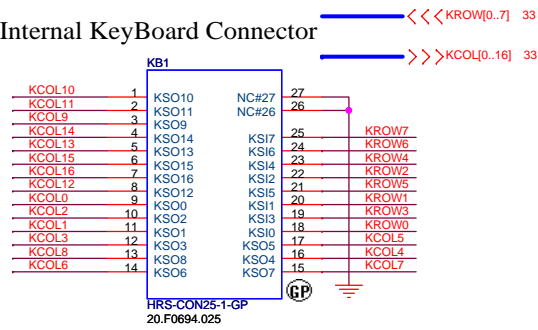
Place these resistors close to connector



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Internal KeyBoard Connector



LED NAME

ACTIVE SIGNAL

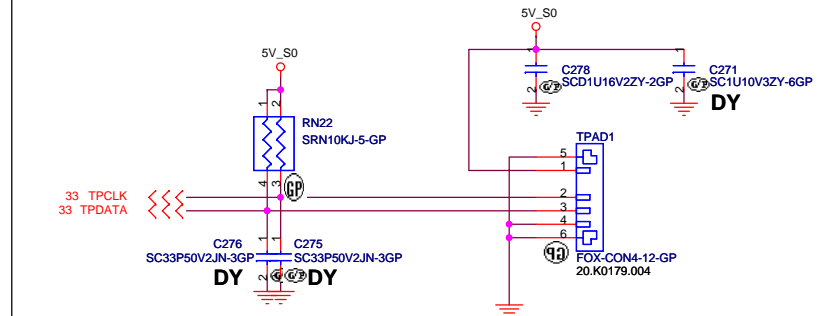
Power Button LED	PWR_BTN_LED
Instant Power Button LED	INST_ON_LED
WLAN LED	WLAN_LED_TEST (from KBC) WLAN_LED# (from Mini)
Bluetooth LED	BT_ACT_WPAN# (from Mini) BT_ACT_K# (from BT)
NUM LED	NUM_LED (from KBC)
SCRLK LED	SCRLK_LED (from KBC)
CAPS LED	CAP_LED (from KBC)

LED Board

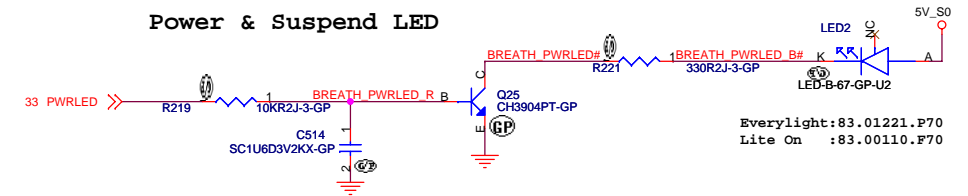
Main Board

Power & Suspend LED	PWRLED (from KBC)
HDD LED	SATA_LED# (from ICH)
Battery LED	BATFULL_LED (from KBC) CHARGE_LED

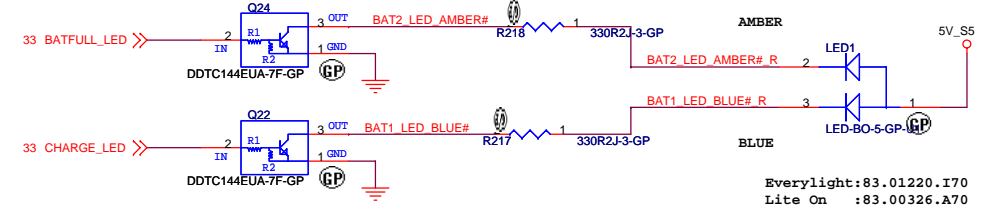
TouchPad Connector



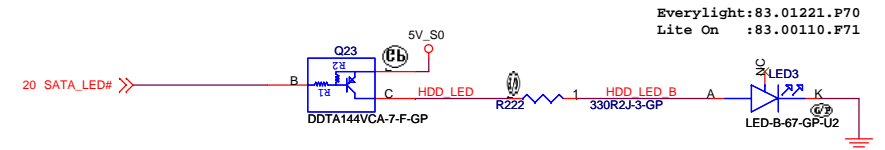
Power & Suspend LED



Battery LED



HDD LED

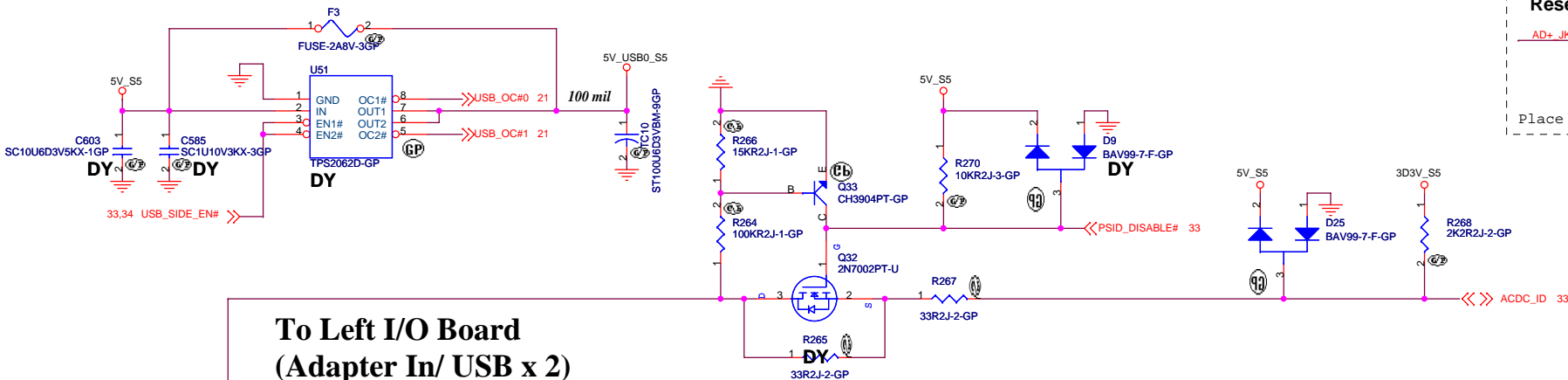


<Core Design>

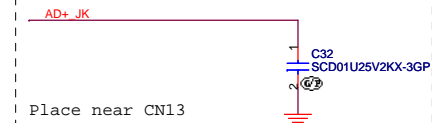
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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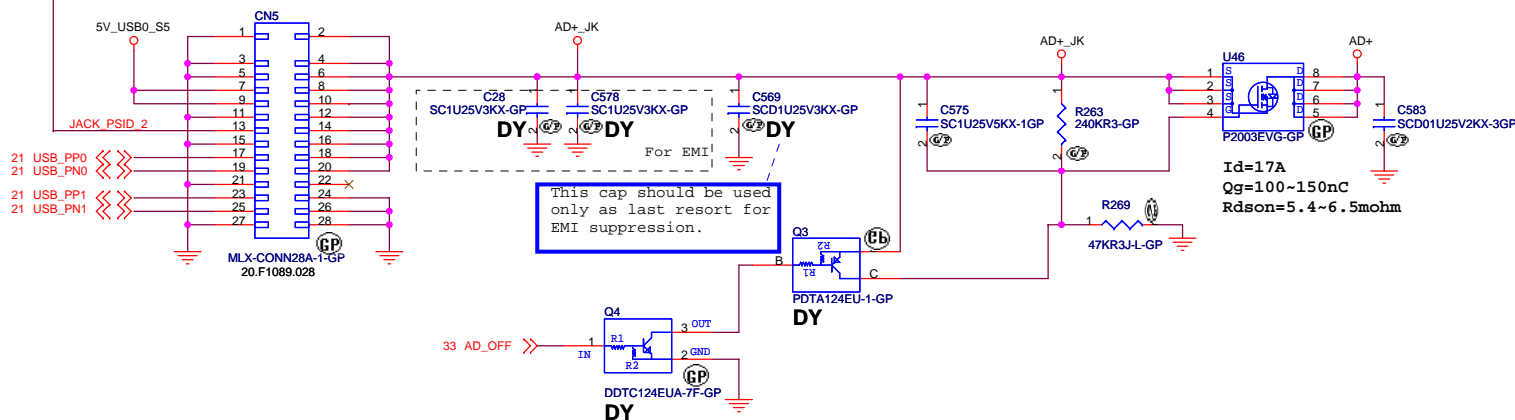
USB POWER



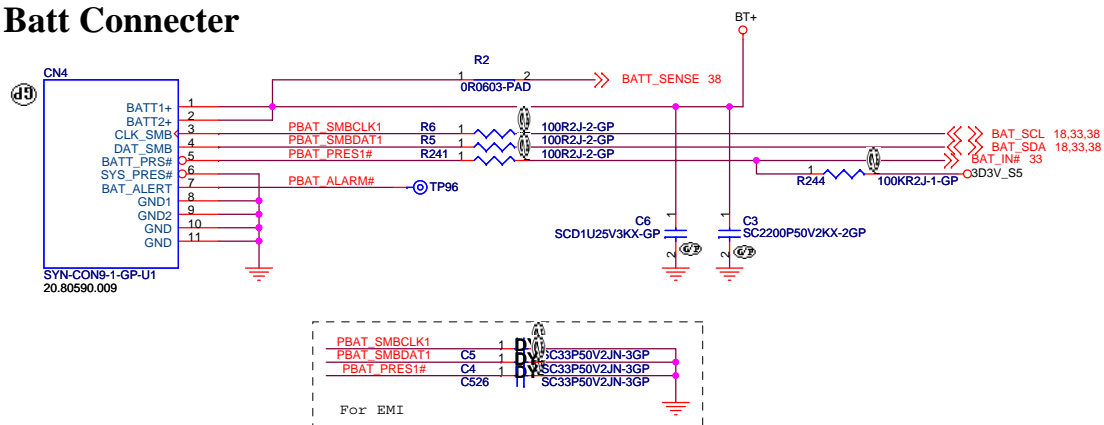
Reserved for EMI



To Left I/O Board (Adapter In/ USB x 2)



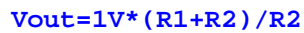
Batt Connector



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Title	Author	Year	Journal	Volume	Page
...

DC to DC 3.3V & 5V

Size	Document Number
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Hawke-Intel

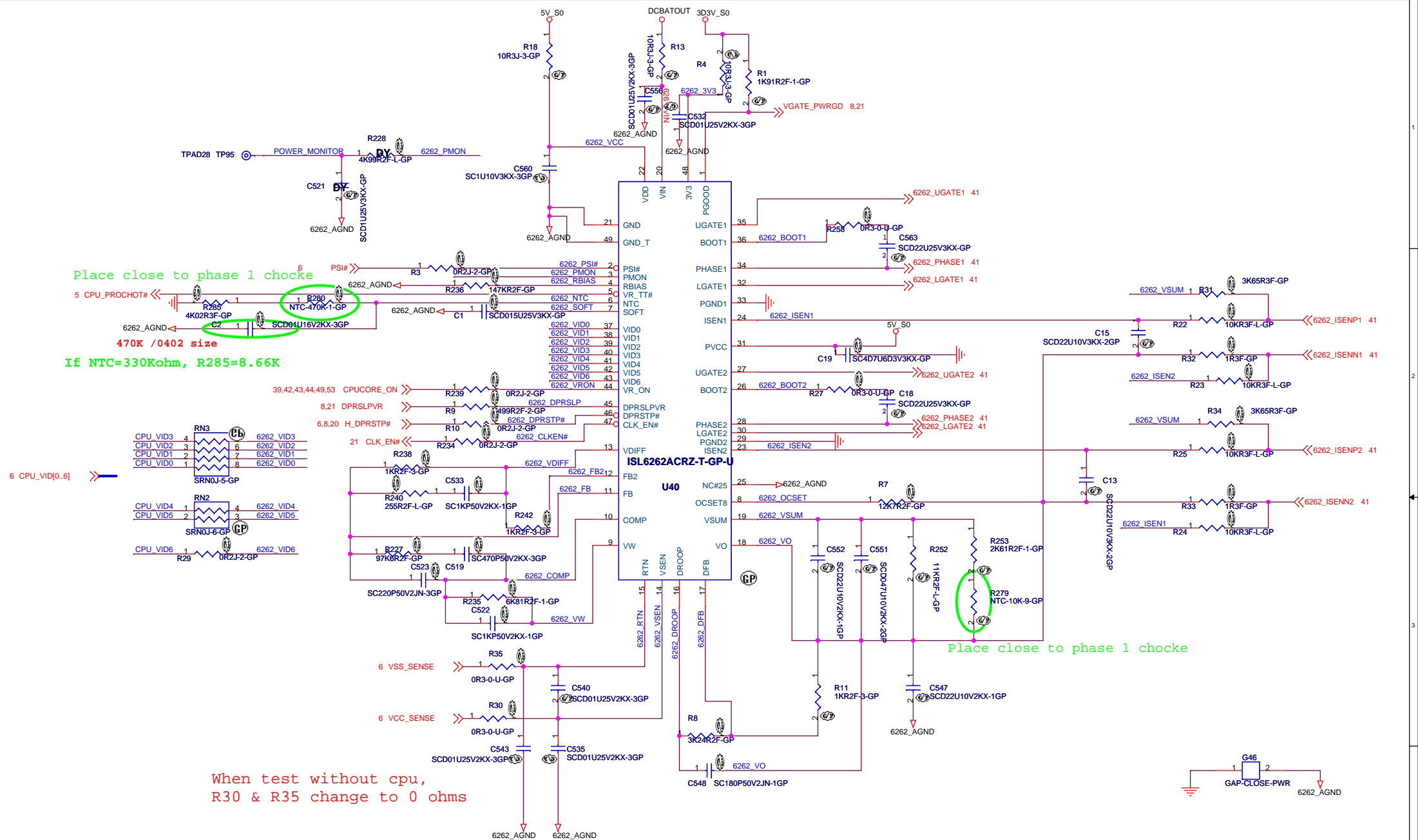
Rev

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Place close to phase 1 choke

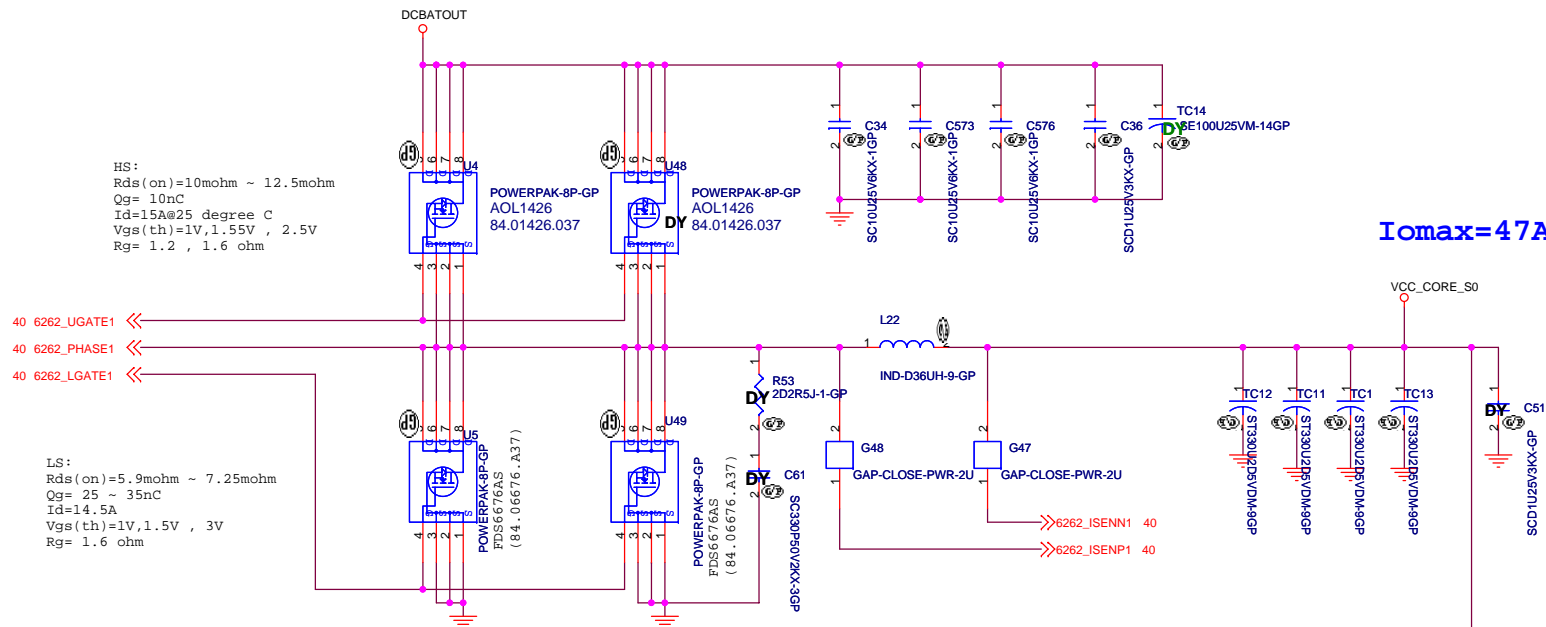
5 CPU_PROCHOT#

470K / 0402 size

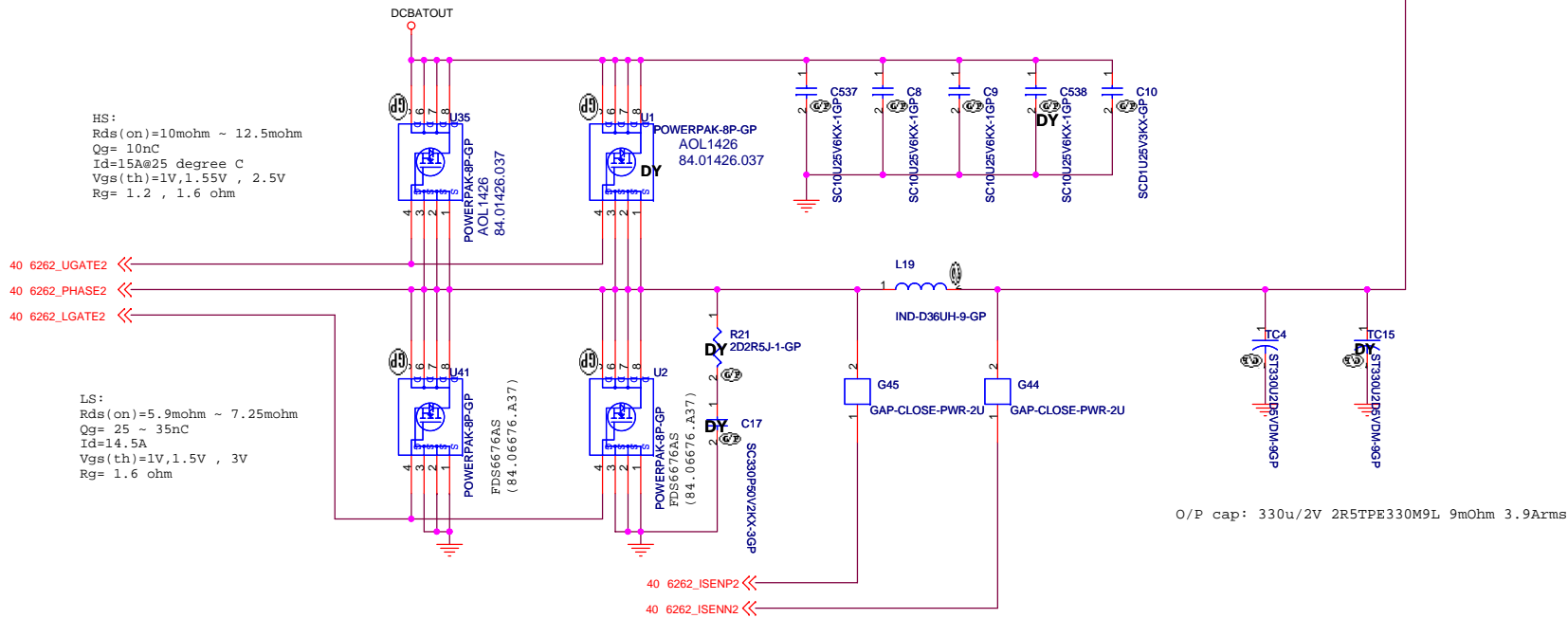
If NTC=330Kohm, R285=8.66K

Place close to phase 1 choke

When test without cpu,
R30 & R35 change to 0 ohms

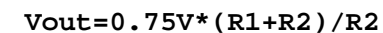


Iomax=47A

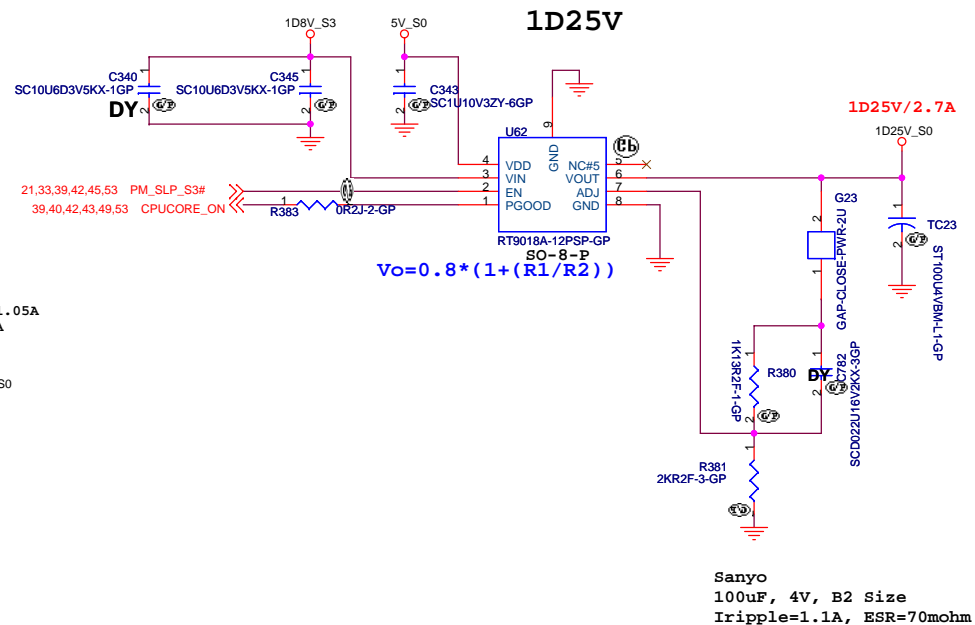
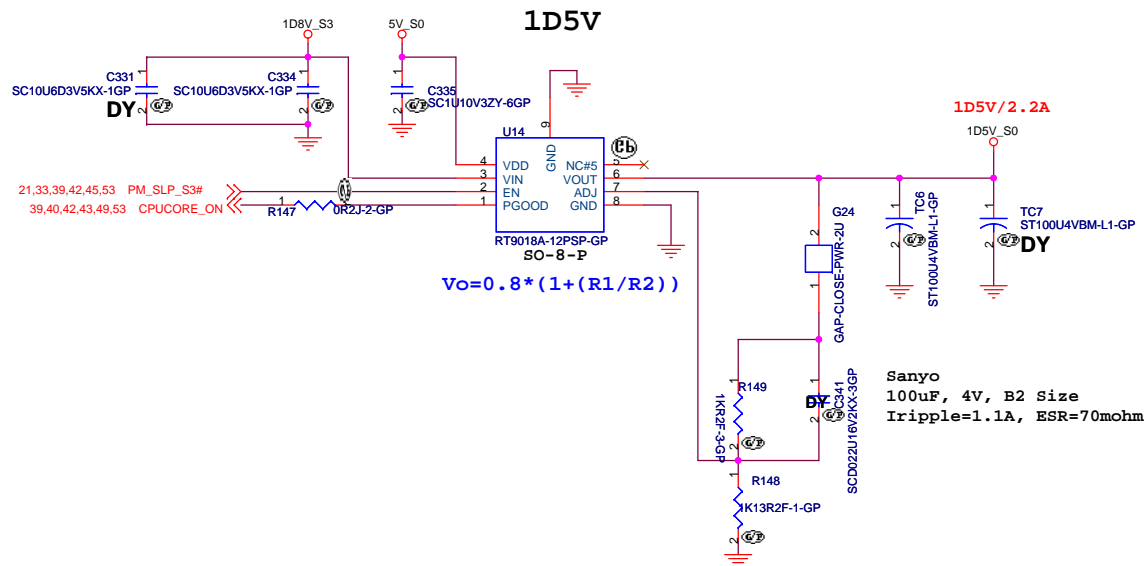


If VCC_SENSE and VSS_SENSE pins have pulled resistors to VCC_CORE_S0
 ==> Remove R44/R45/R46/R47.

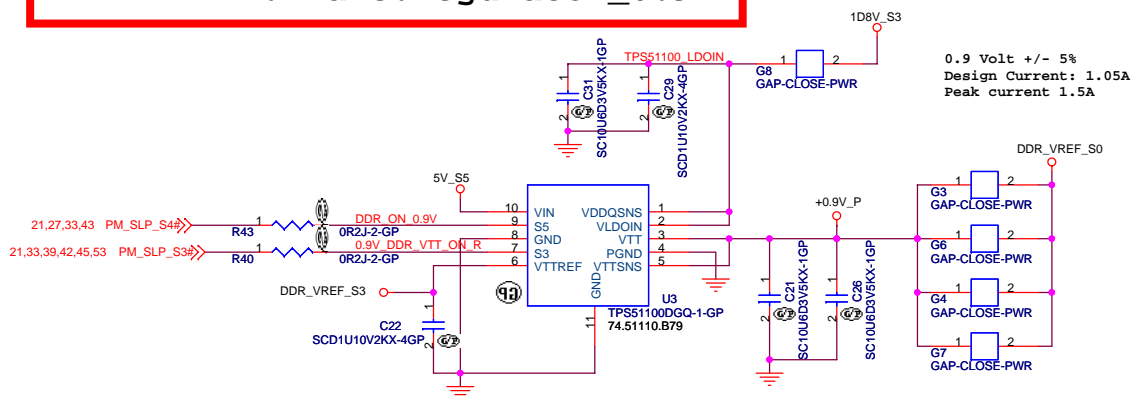
<Core Design>



Title			
DC/DC 1D8V(ISL6268)			
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Hawke-Intel			
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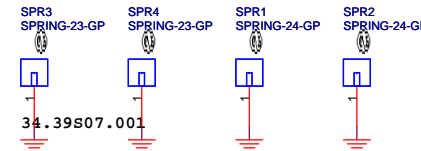
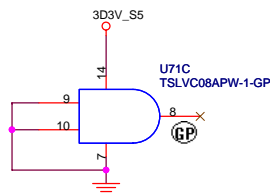
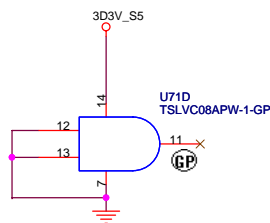
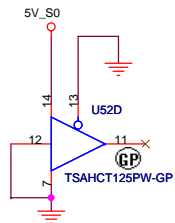
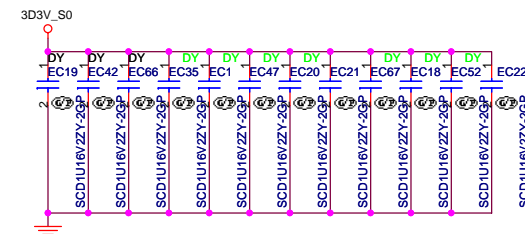
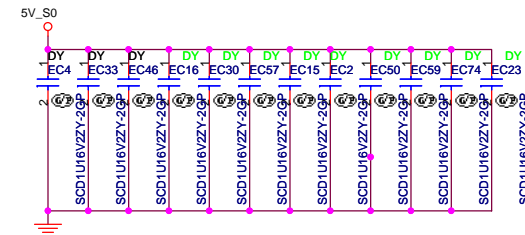
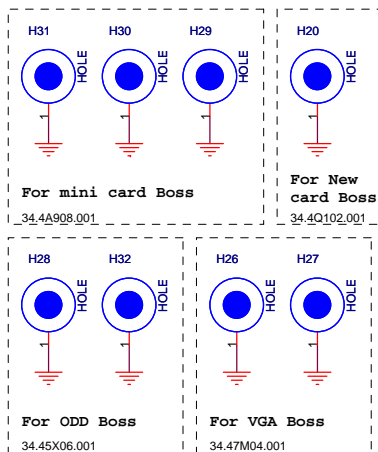
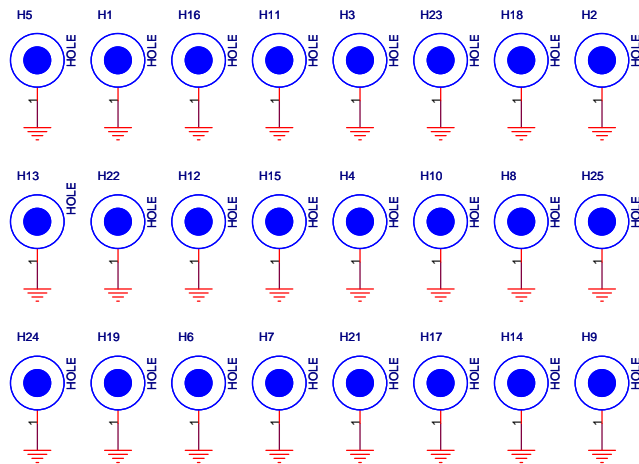
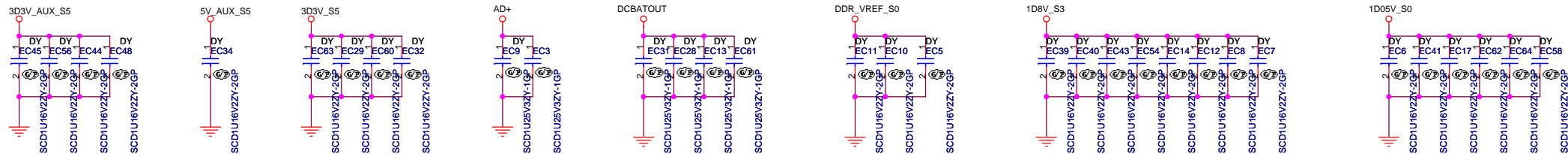


SSID = PWR.Plane.Regulator_0.9V



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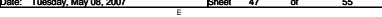
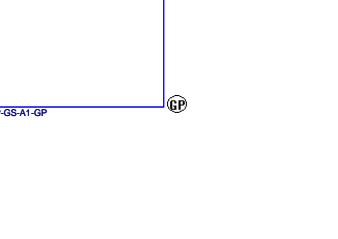
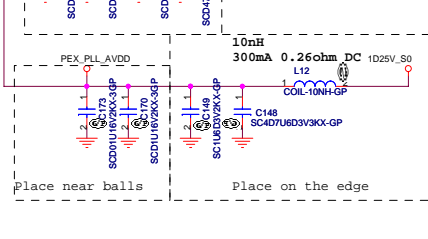
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
DC to DC 1D5V / 0D9V /1D25V		
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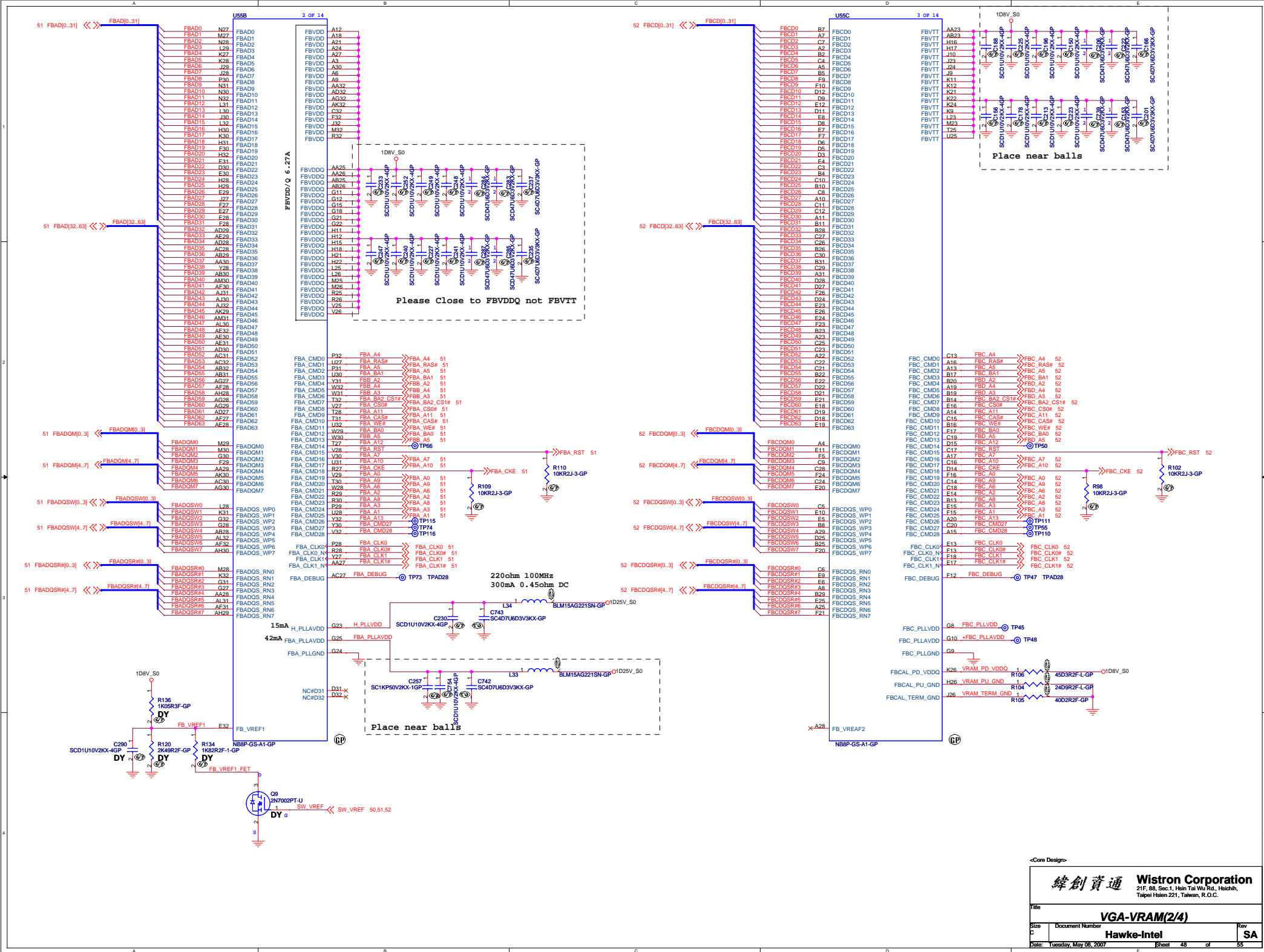


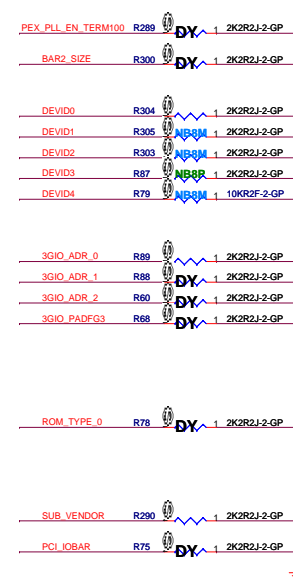
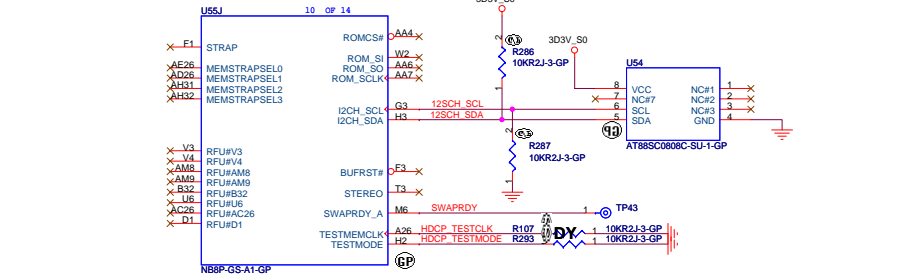
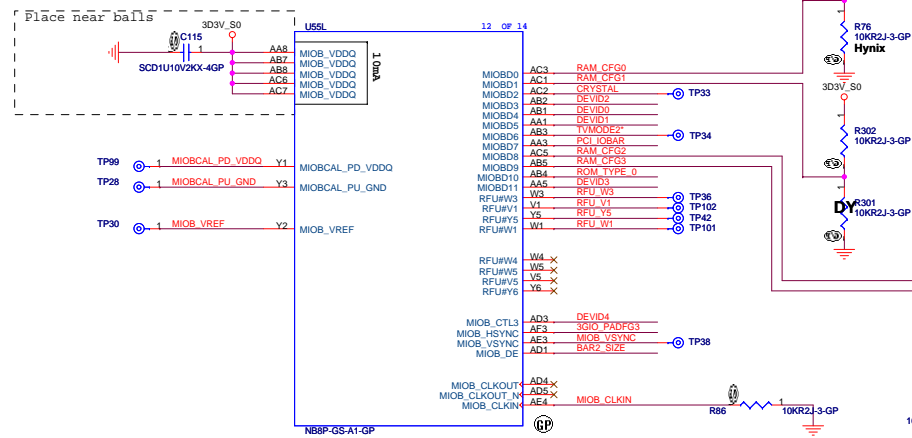
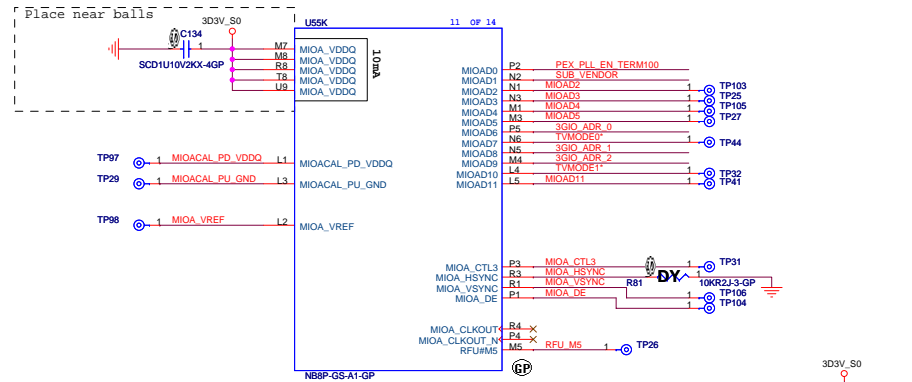
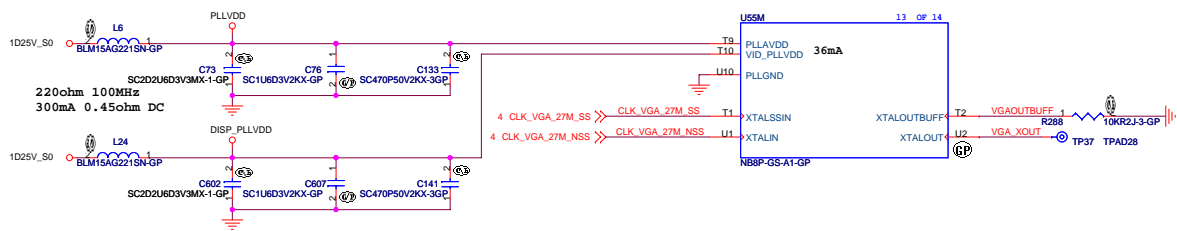
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title			MISC	
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PEX_PLL_EN_TERM100		BAR2_SIZE	
0	Enable	0	32 Mb
1	Disable	1	16 Mb

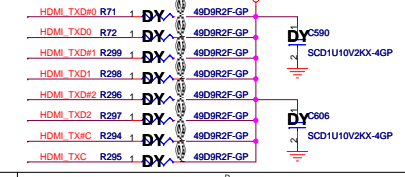
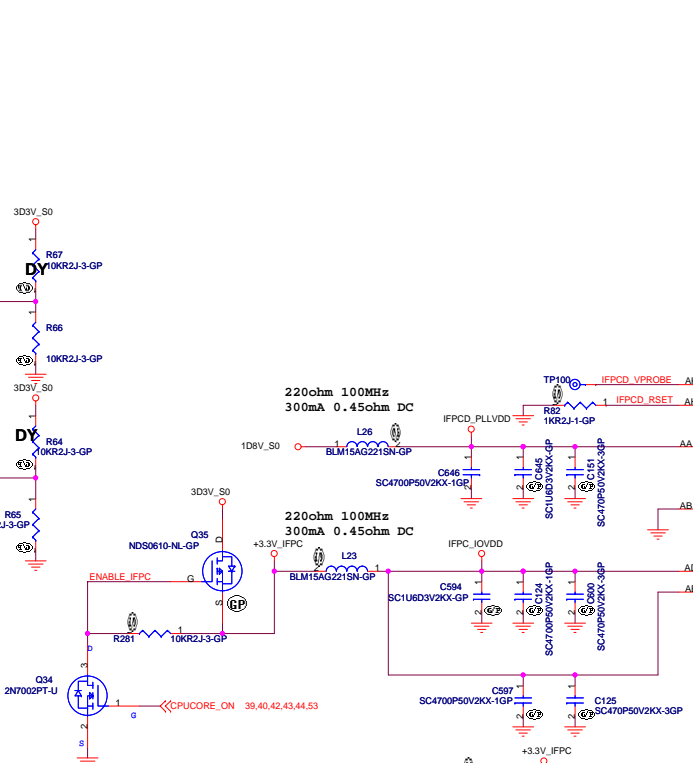
DEVID0	DEVID1	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	1	0	0
G72M	1	1	0	0	0
G72MV	1	0	1	1	1
G86M	1	0	1	1	1
G84	0	1	0	0	1

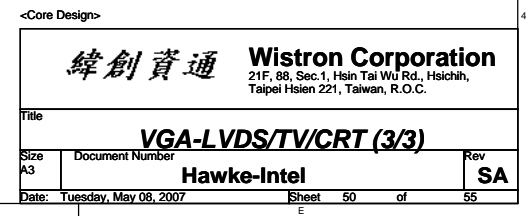
3GIO_PADCFG[3:0]		Notes
0000	Desktop	(Default)
0001	Mobile1	Recommended for NV43/NV44/G7x
0010	Mobile2	NV42
0011	Mobile3	
0100	Reserved	
0101...1110	Reserved	
1111	Reserved	

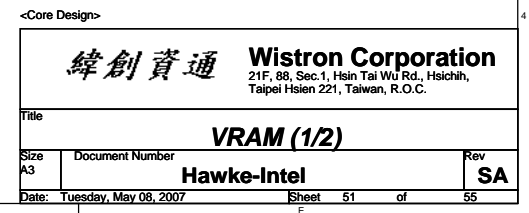
ROMTYPE[1:0]	
00	Parallel
01	Serial
10	Reserved
11	LPC

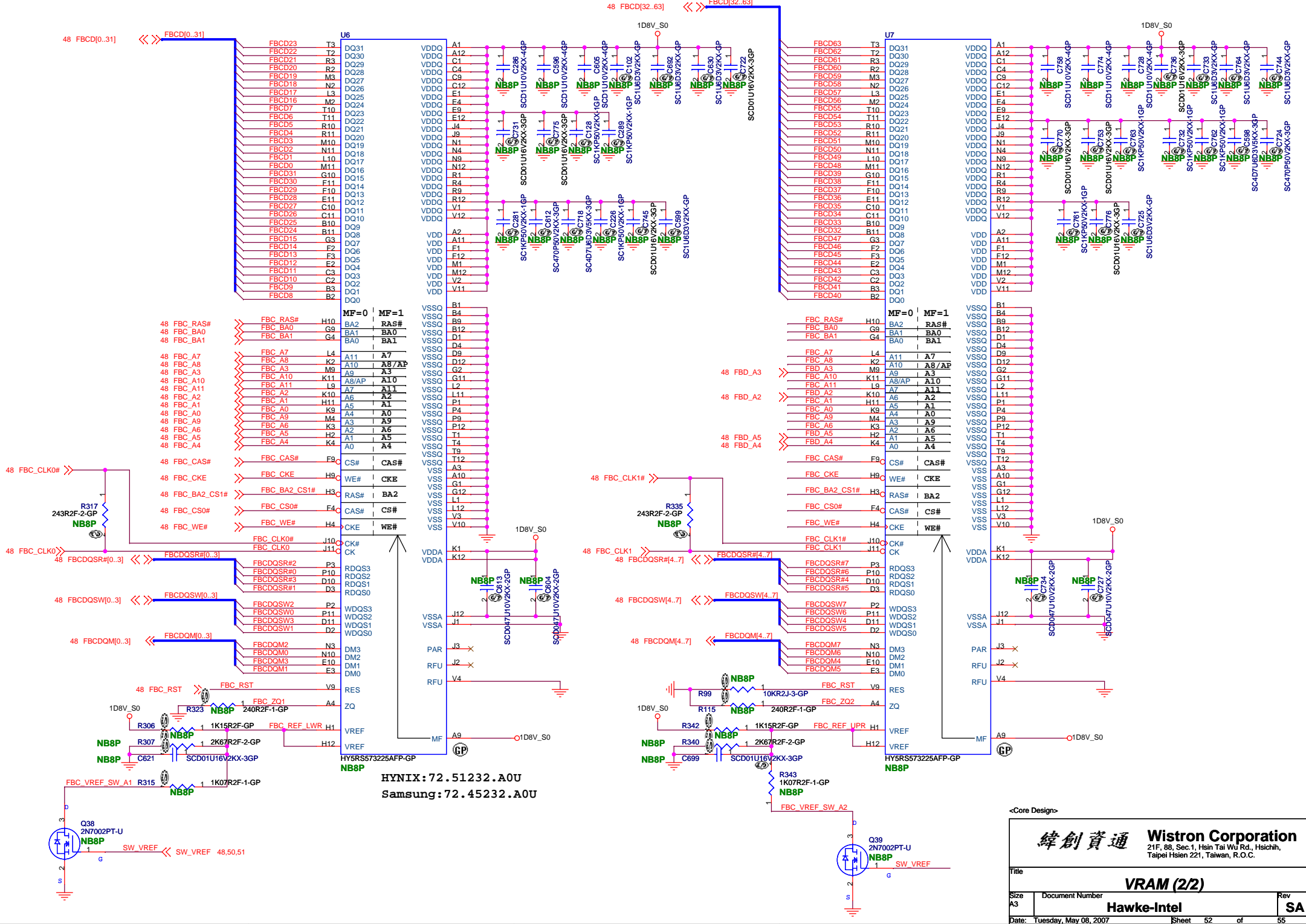
SUB_VENDOR		PCI_IOBAR	
0	No video BIOS ROM	0	Disabled
1	BIOS ROM is present	1	Enabled

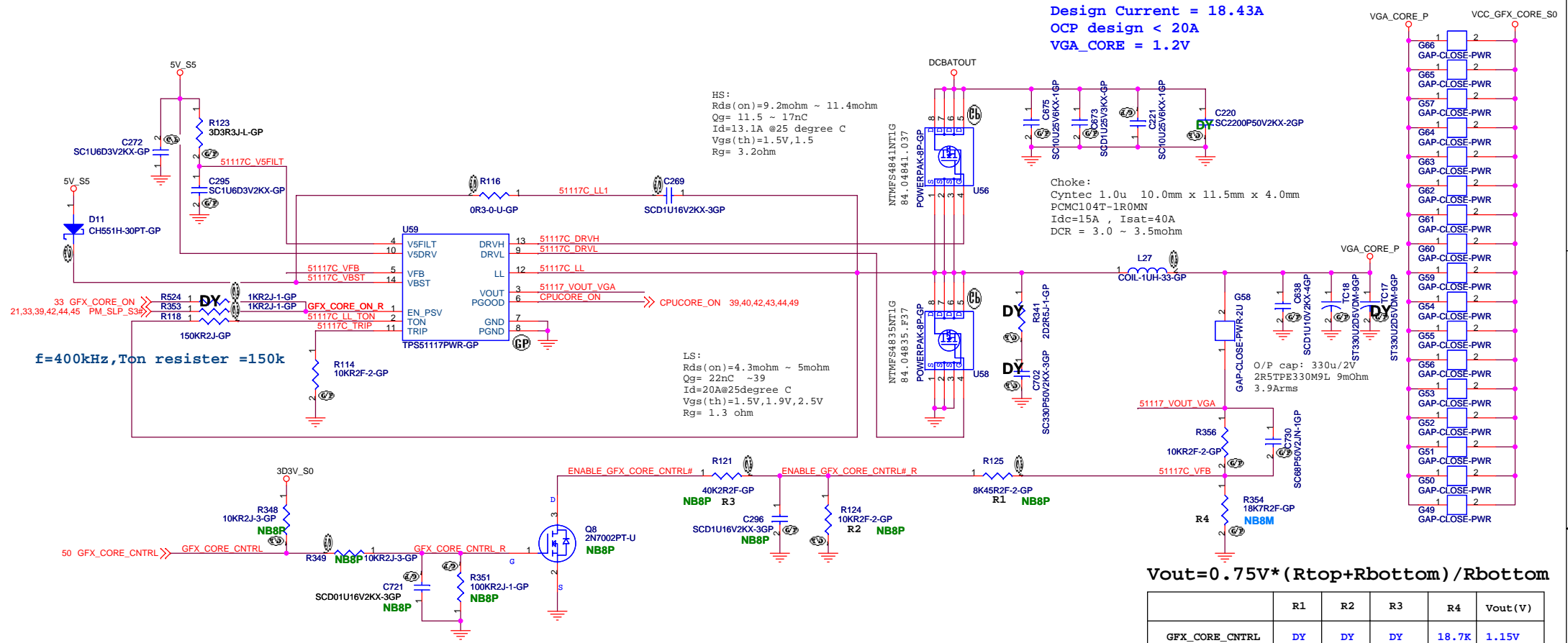
RAM_CFG[3:0]		
MIOBD0	Infineon 8MX32	0101
MIOBD1	DDR3 1.8V	
MIOBD2	Hynix 8MX32	0111
MIOBD3	DDR3 1.8V	
MIOBD4	Samsung 8MX32	0110
MIOBD5	DDR3 1.8V	
MIOBD6	Infineon 16MX32	0001
MIOBD7	DDR3 1.8V	
MIOBD8	Hynix 16MX32	0010
MIOBD9	DDR3 1.8V	
MIOBD10	Samsung 16MX32	0011
MIOBD11	DDR3 1.8V	



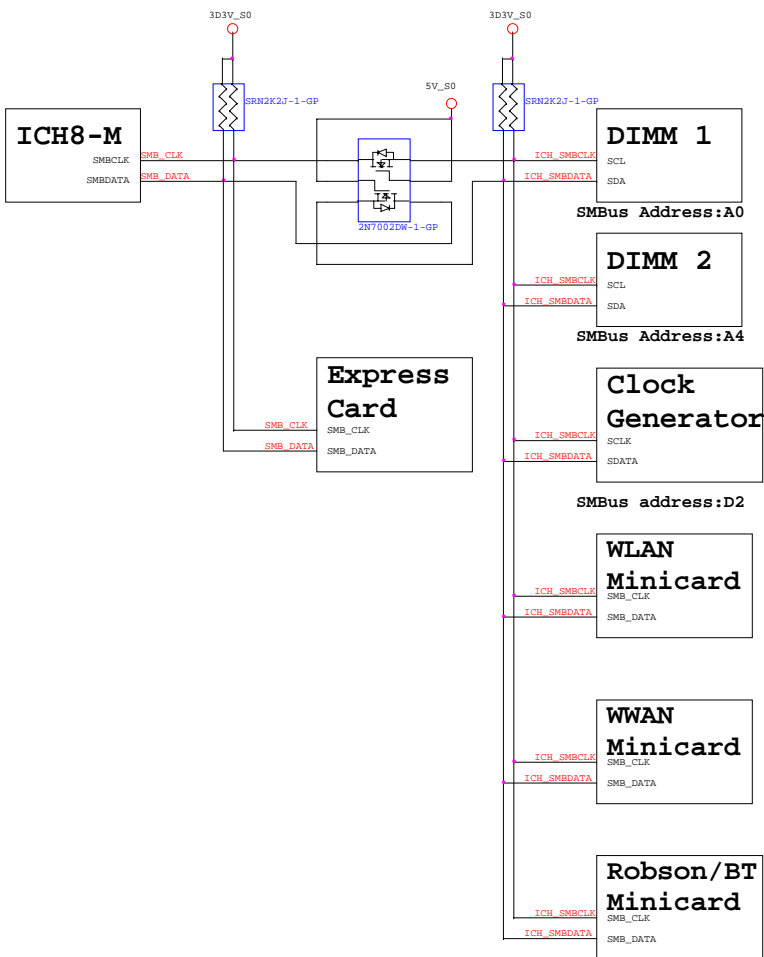




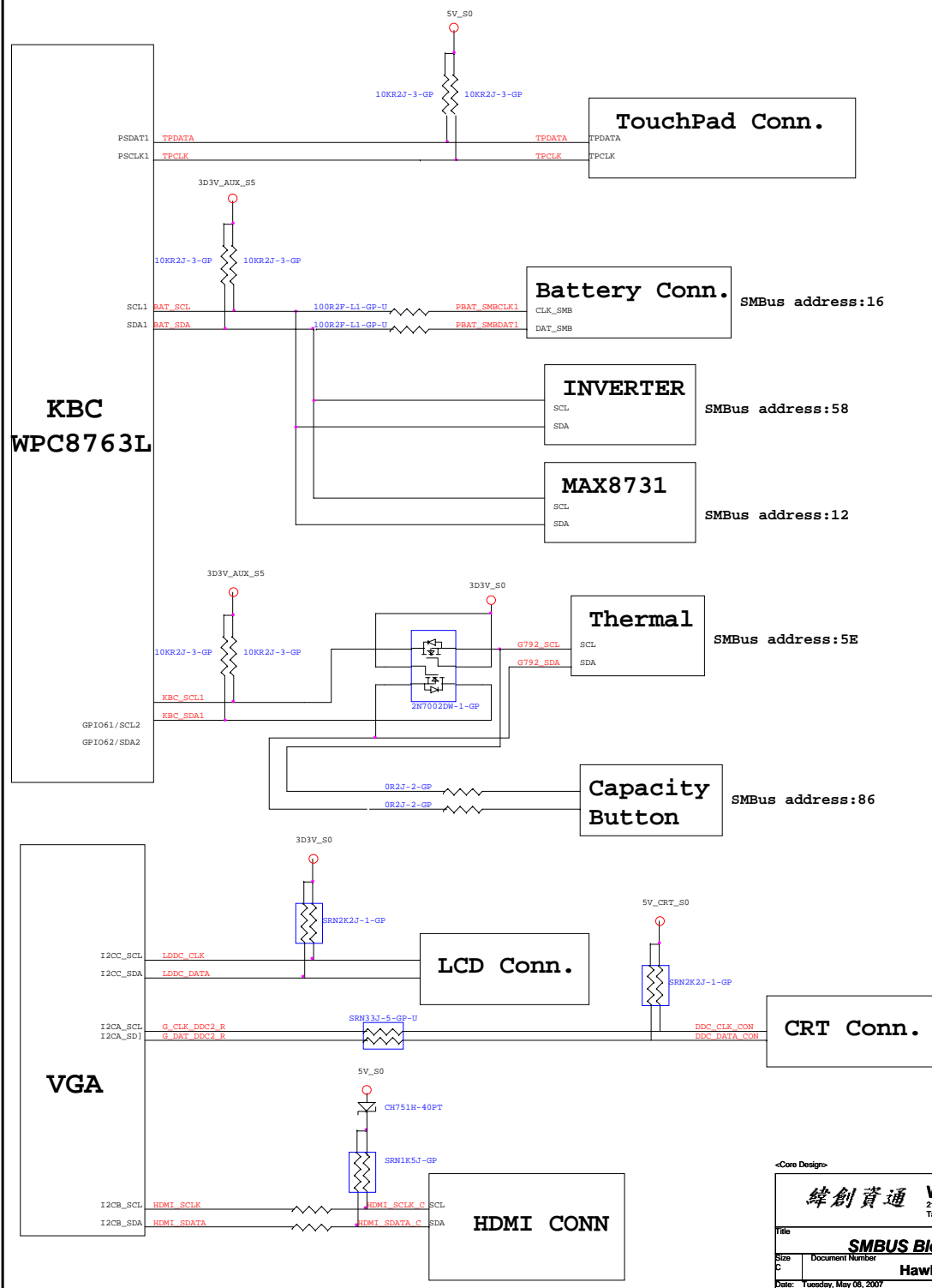




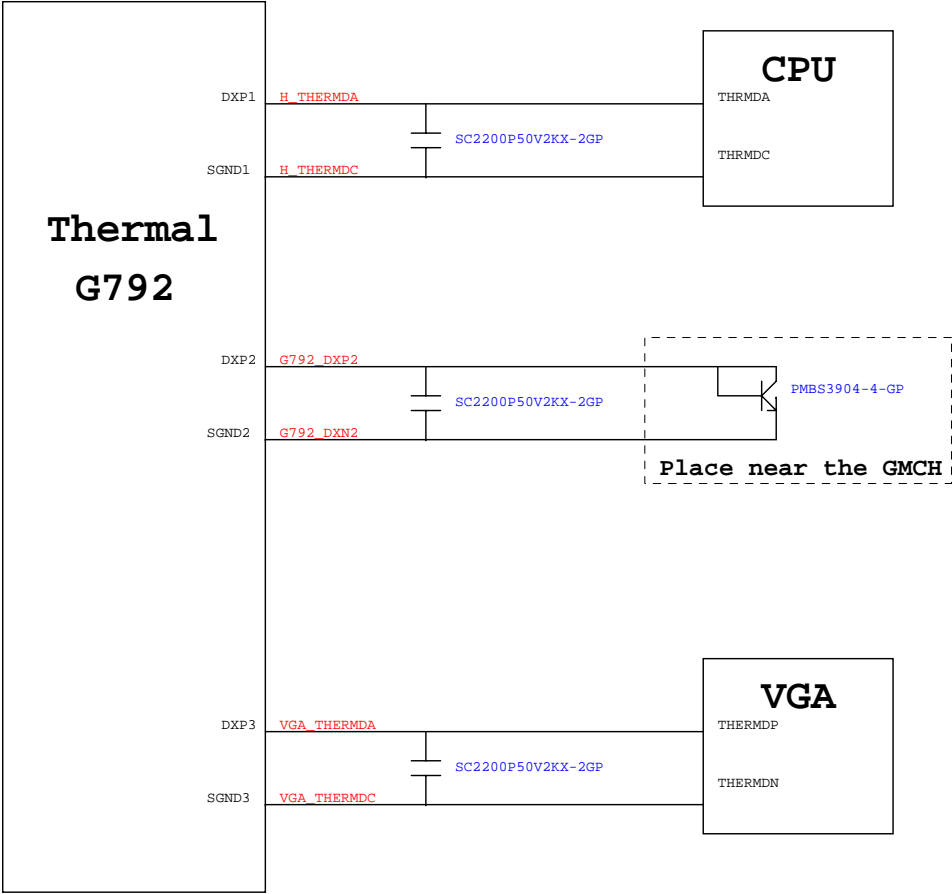
ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

